Compal Confidential

A4WAS MB Schematic Document

LA-C611P

Rev: 1.0

2015.07.17

DAX

Part Number	Description
DAZ1DR00100	PCB A4WAS LA-C611P LS-C341P

A4WAS_PCB_REV10

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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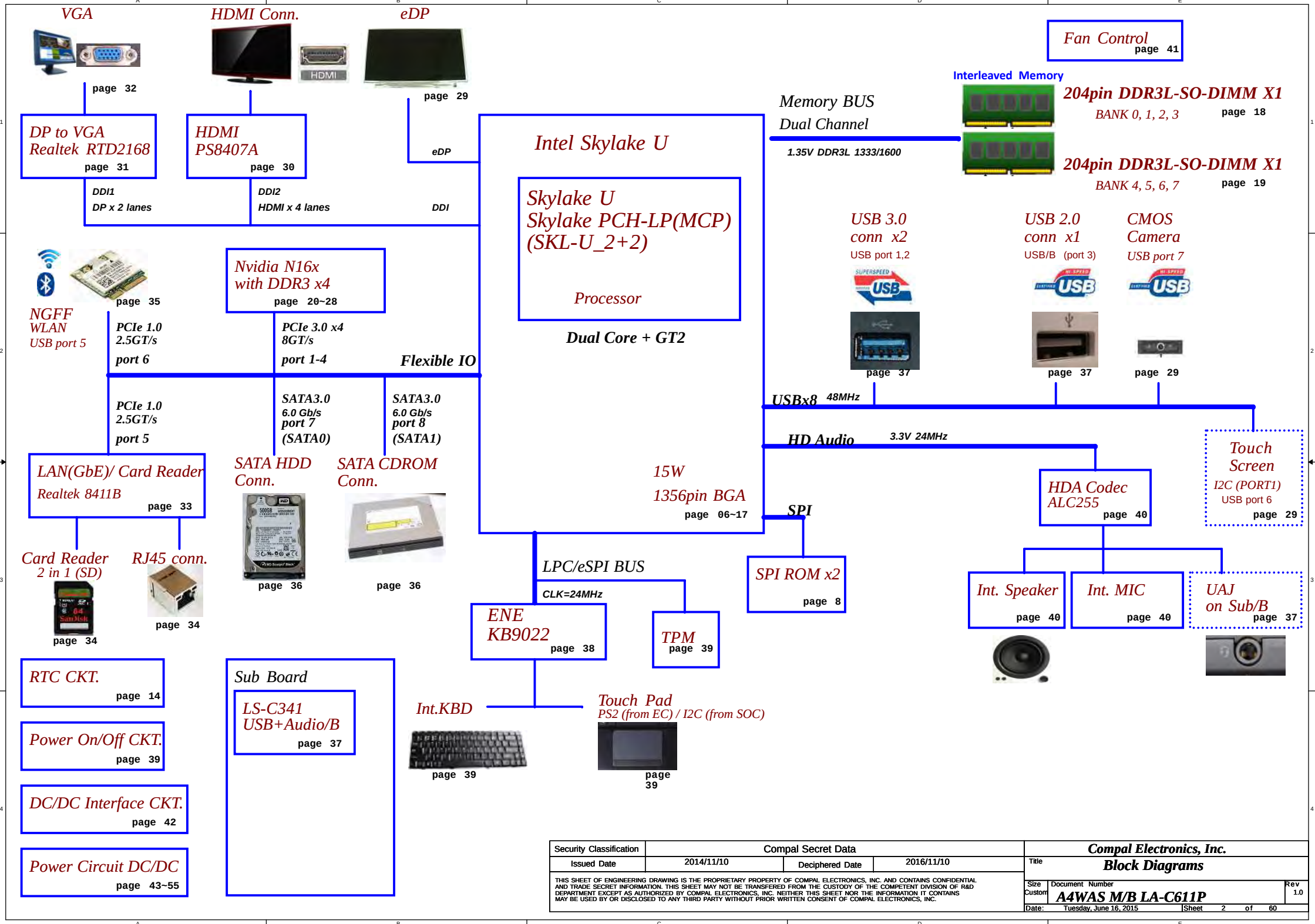
Title: Cover Sheet

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Friday, July 17, 2015 | Sheet 1 of 60



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Title: **Block Diagrams**

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
CODEC(ALC255)	255@
CODEC(ALC283)	283@
SPI ROM 8M*2	8M_DUAL@
SPI ROM 8M*1	8M_SINGLE@
UMA only	UMA@
TPM	TPM@
For Intel CMC	CMC@
For ES Sampel Only	ES@
Keyboard backlight	KB@
LPC MODE for EC	LPC@
ESPI MODE for EC	ESPI@
BA Serial	BA@
EA Serial	HDD@

BOM Option Table

Item	BOM Structure
dGPU	VGA@
N16S-GT	SGT@
N16V-GM SKU	VGM@
GPU CG6 / Non GC6	NGC6@ / GC6@
VRAM BOM Select	X76@/X7601@ ~ X7614@
Single/Dual Rank	SR@/DR@
Memory Door/ No Memory Door	MDY@/ MDN@
DMIC*1	1DMIC@
DMIC*2	2DMIC@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
CPU Code	PreES:QH7Y@ ES:QHMF@, QHMG@ QS:QJFC@, QJ8N@, QJ8L@ MP:SR2EU@, SR2EY@, SR2EZ@

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.675VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.35V_VDDQ	DDRIIIL +1.35V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

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Compal Electronics, Inc.

Title: Power Map

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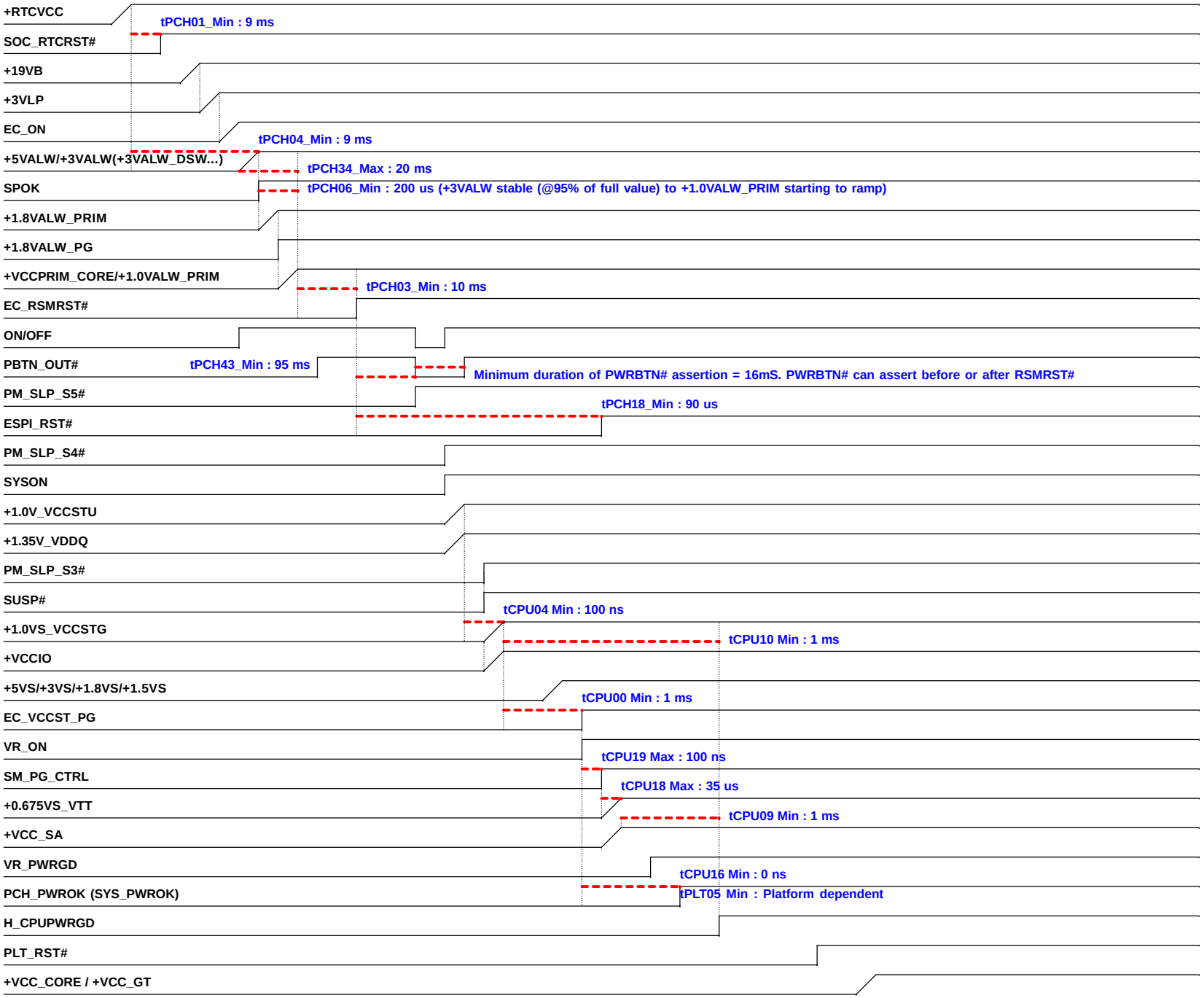
PWR Sequence_SKL-U2+2_DDR3L_NON CS



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Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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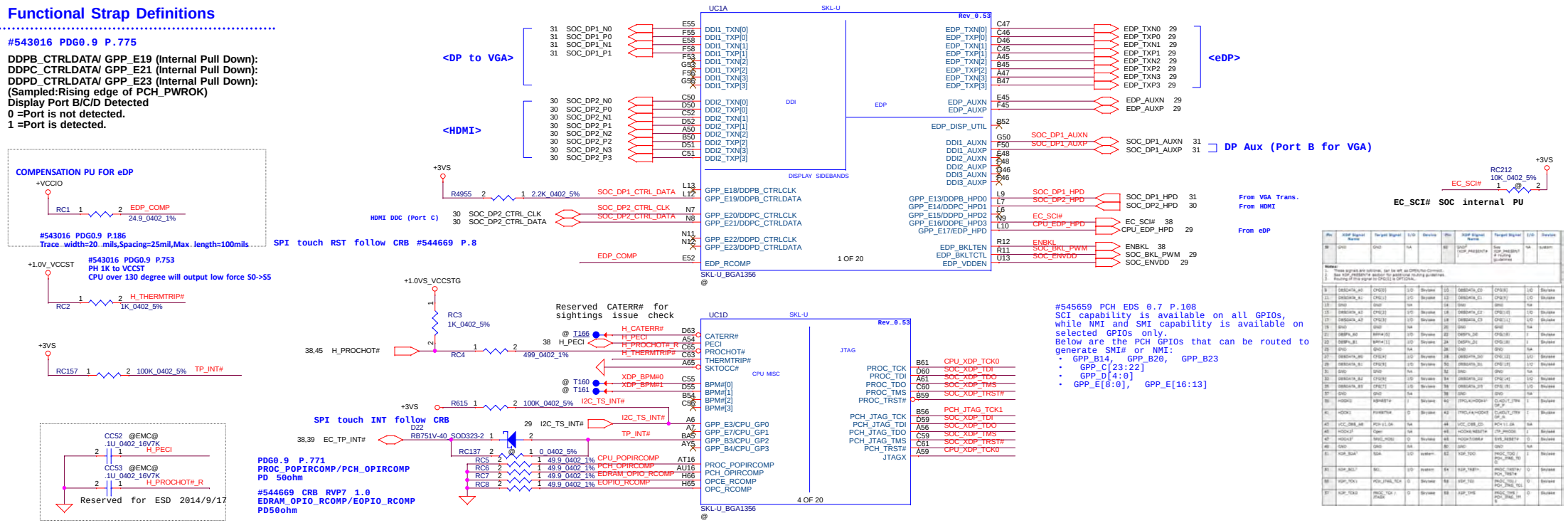
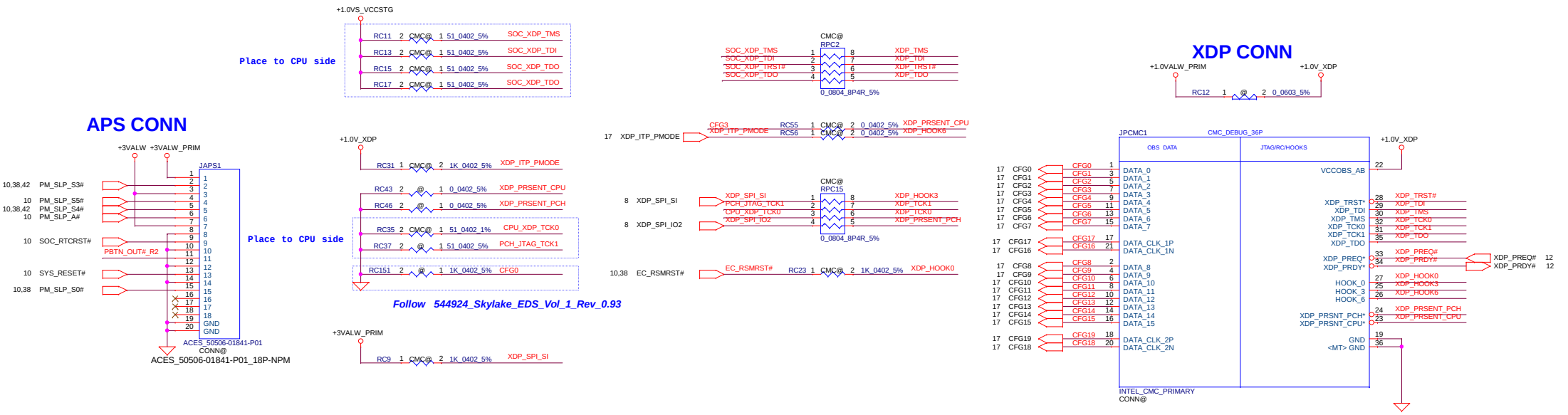
Functional Strap Definitions

#543016 PDG0.9 P.775

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.





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Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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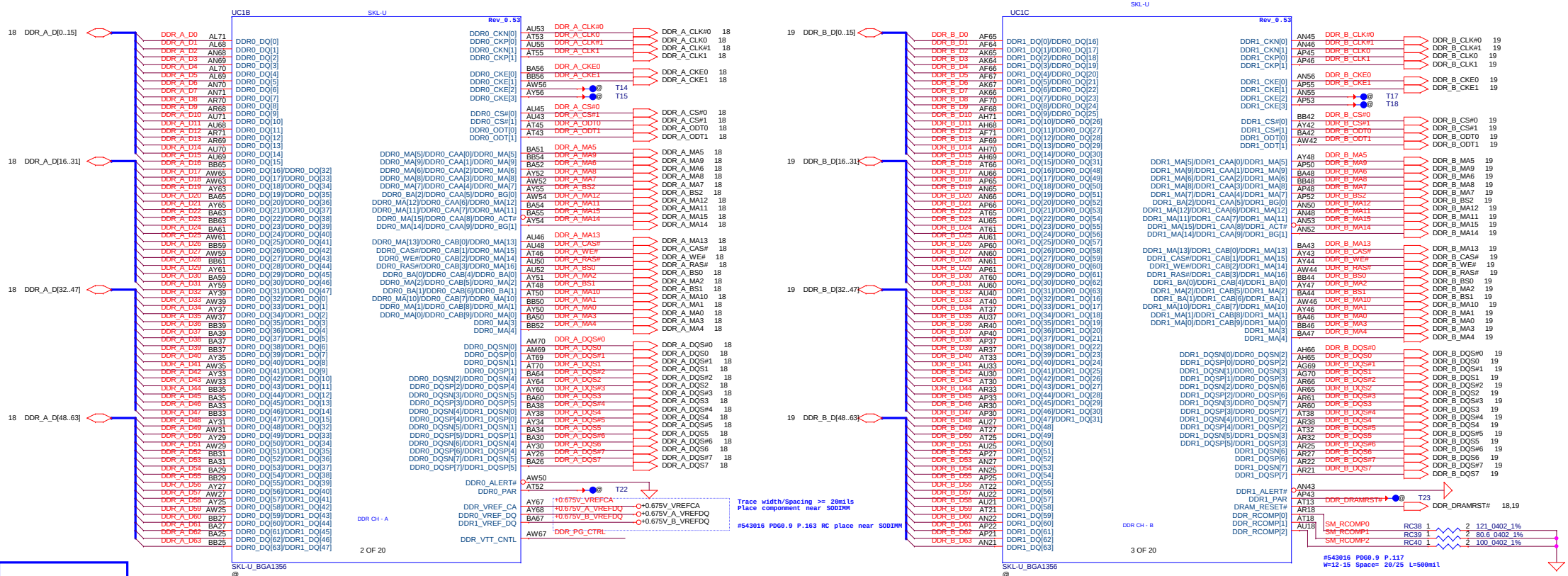
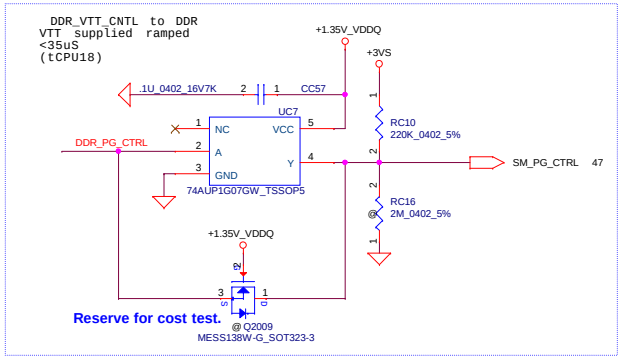
Interleaved Memory





Pre_ES Sample

UC1

CPU_QH7Y_A2_1.6G
QH7Y@
SA00008A400

ES Sample

UC1

CPU_QHMF_C0_2.3G
QHMF@
SA00008M420

UC1

CPU_QHMG_C0_1.6G
QHMG@
SA00008M320

QS Sample

UC1

CPU_ i3-6100U_D0_2.3G
QJFC@
SA000092N30

UC1

CPU_i5-6200U_D0_2.3G
QJ8N@
SA000092O30

UC1

CPU_i7-6500U_D0_2.5G
QJ8L@
SA000092P20

MP Sample Add on 7/14

UC1

CPU_ i3-6100U_D1_2.3G
SR2EU@
SA000092NB0

UC1

CPU_i5-6200U_D1_2.3G
SR2EY@
SA000092OB0

UC1

CPU_i7-6500U_D1_2.5G
SR2EZ@
SA000092P90

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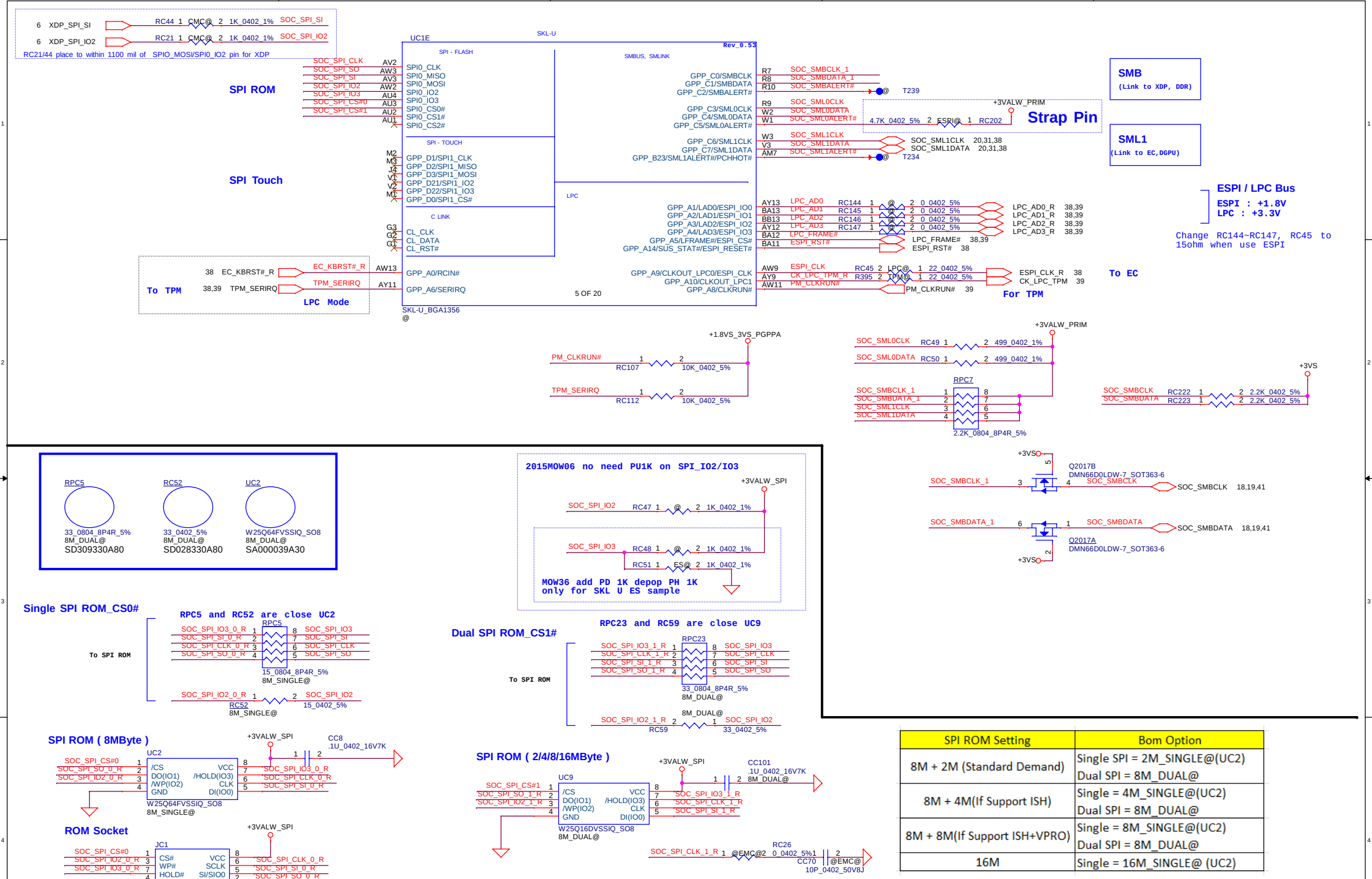
Compal Electronics, Inc.

Title: SKL-U(2/12)DDRIII

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, July 14, 2015 | Sheet 7 of 60



SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

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Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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#545659 SKL_PCH_EDS_R0.7 P.84

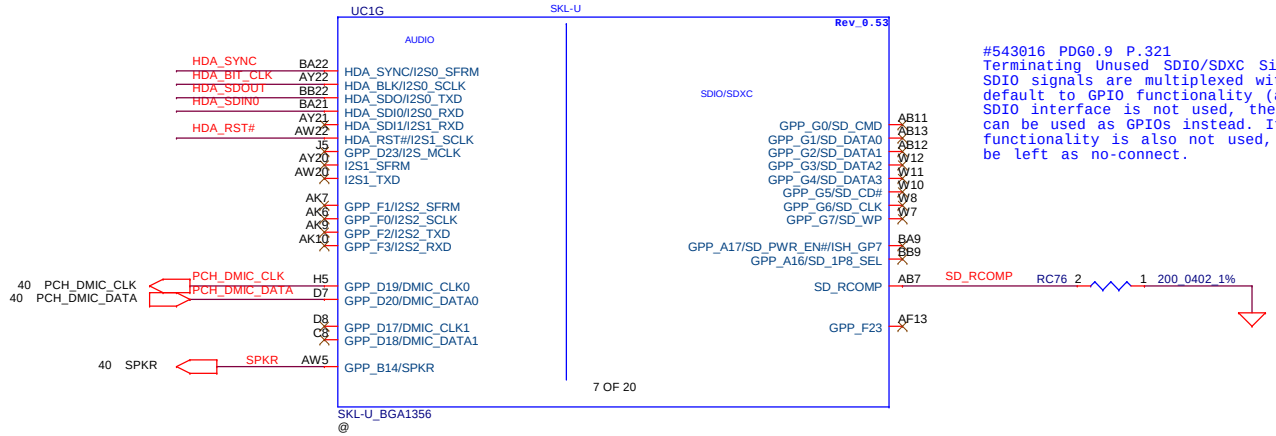
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
  - SDO double pumped up to 48 Mb/s
  - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.



#543016 PDG0.9 P.321
Terminating Unused SDIO/SDXC Signals
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

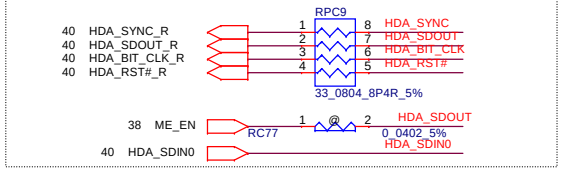
62.3.38 RCOMP Checklist

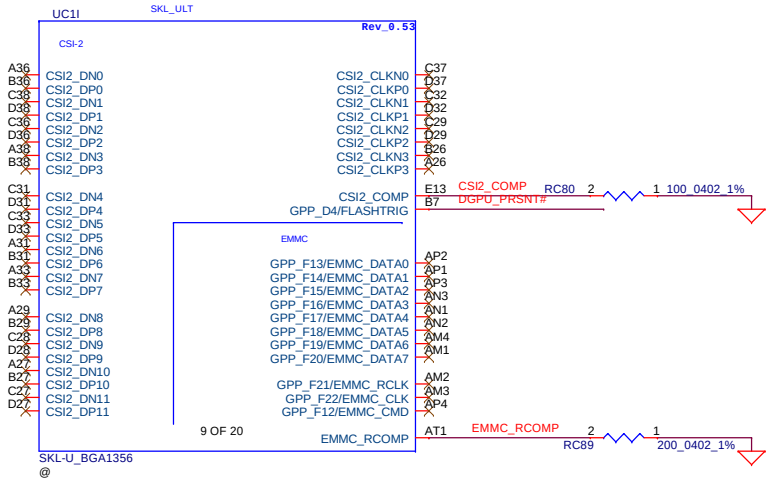
Table 62-48. RCOMP Checklist

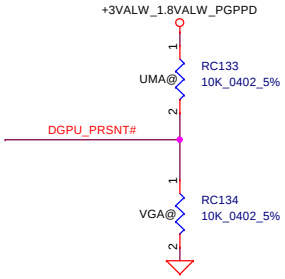
Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_COMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

HDA for AUDIO







	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

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Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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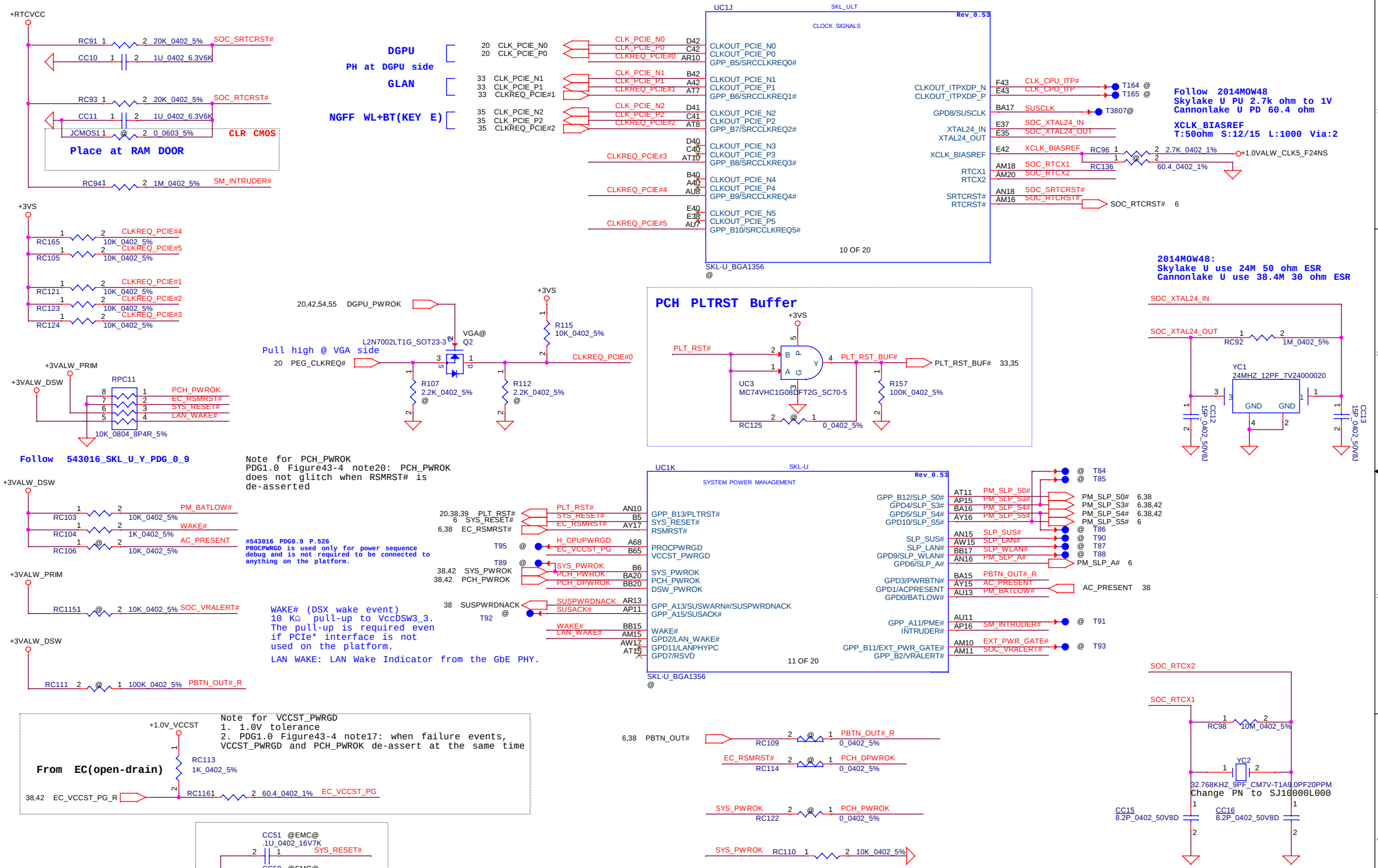

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Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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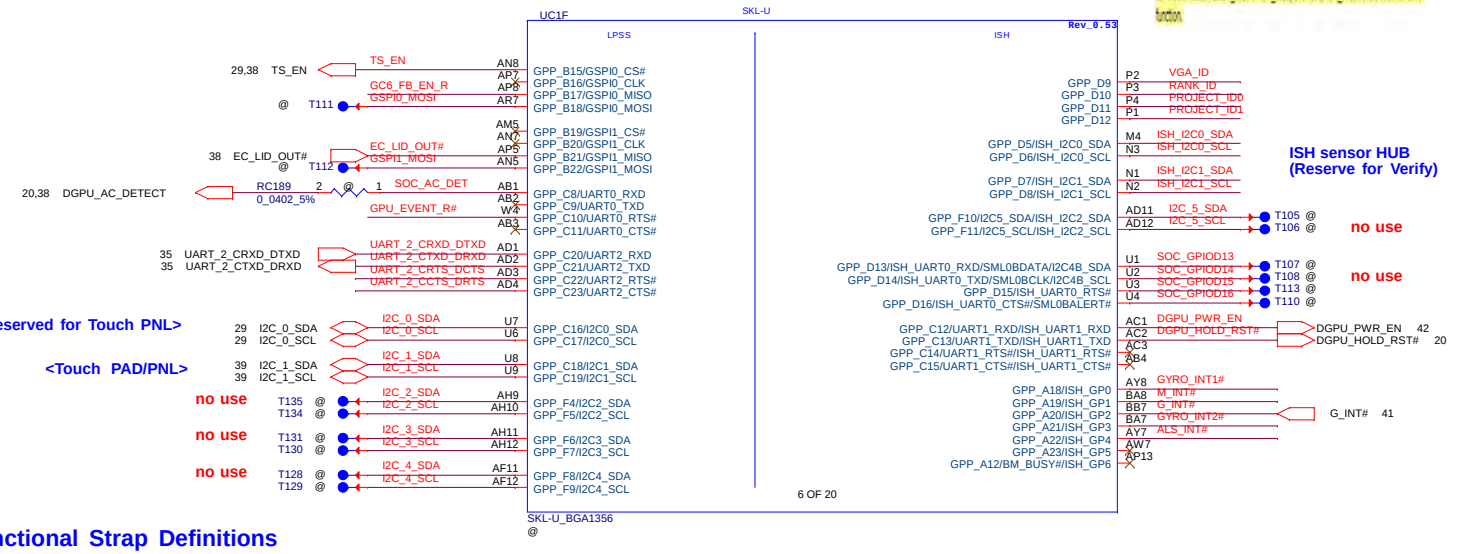
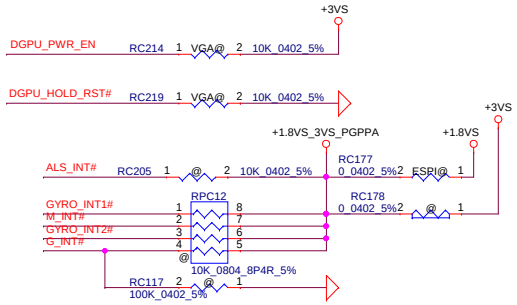
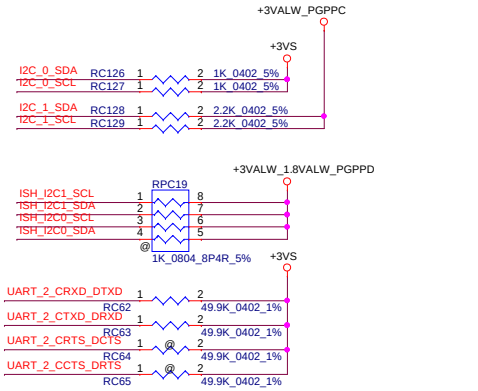
543016 SKY PDG 0.9 P.401

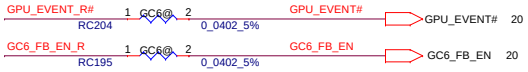
The sensors are connected to ISH through ISH I2C interface and ISH GPIO. Sensors can be connected to ISH_I2C0 or ISH_I2C1, but not to ISH_I2C2 as it is used for other function



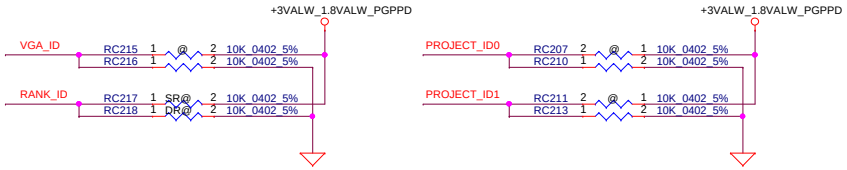
ISH sensor HUB
(Reserve for Verify)







TO DGPU



Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
* 0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

* 0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
* 0 = SPI Mode --> AAX05 Use
1 = LPC Mode

SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
* 0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
* 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

VGA_ID	GPP_D9
GL	0
GM	1

RANK_ID	GPP_D10
DR	0
SR	1

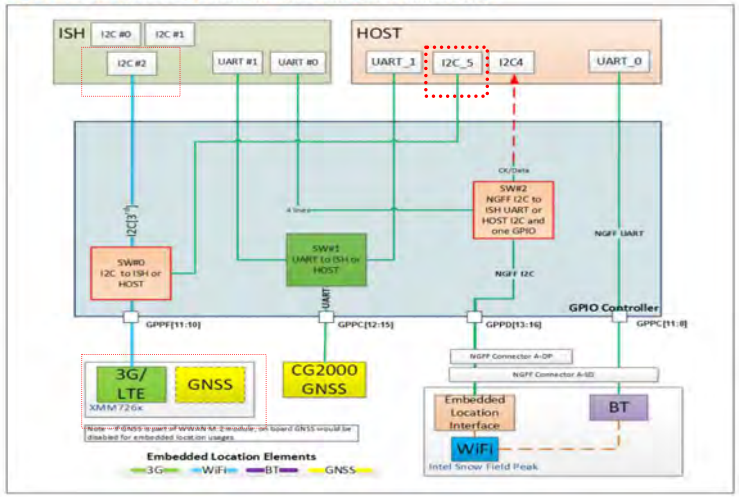
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*A4WAS	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

HDA_SDO/I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port D is not detected.
1 =Port D is detected.

I2C/ISH Port(From PDG 0.9)

Figure 64-1. Embedded Location - Host and ISH Connectivity



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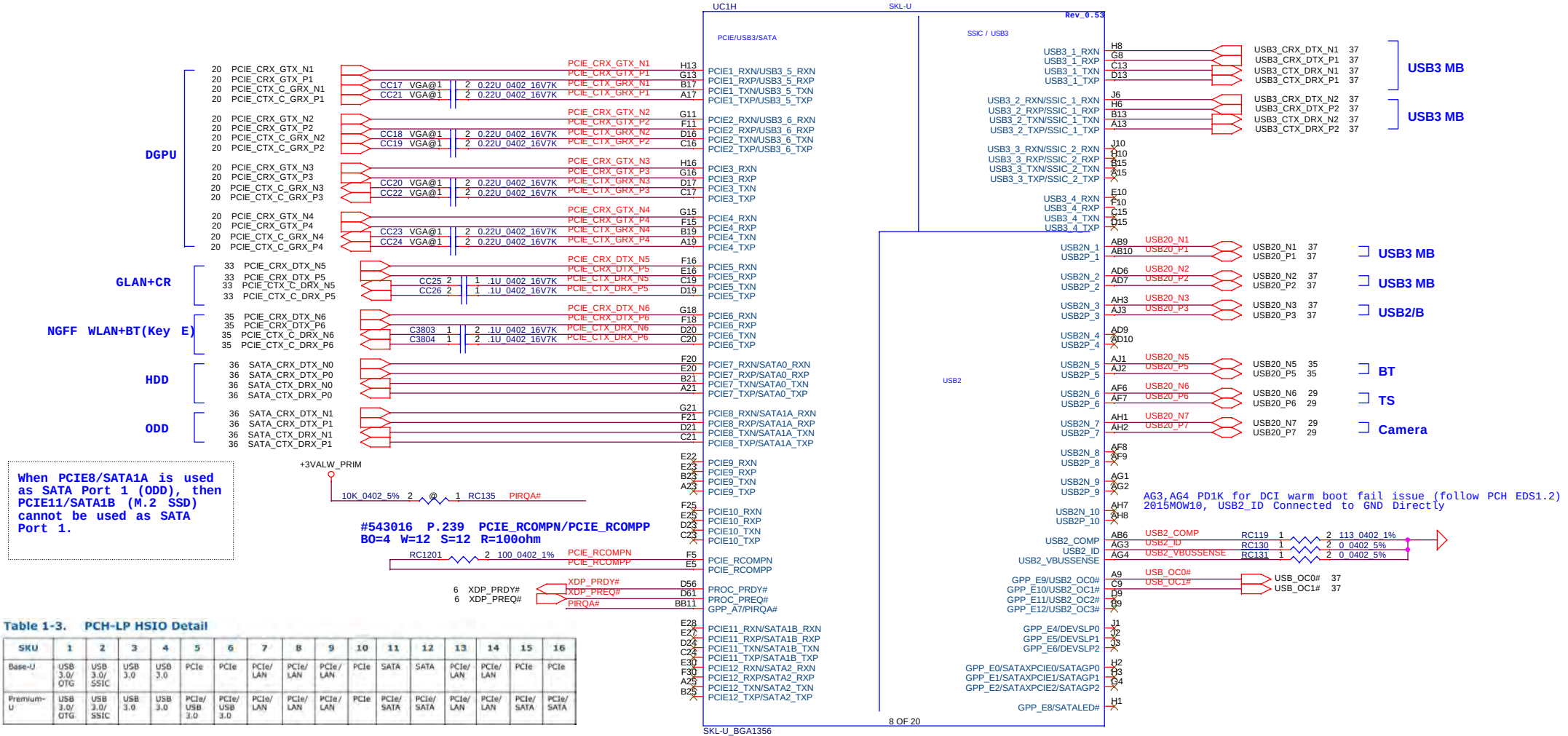
Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 11 of 60

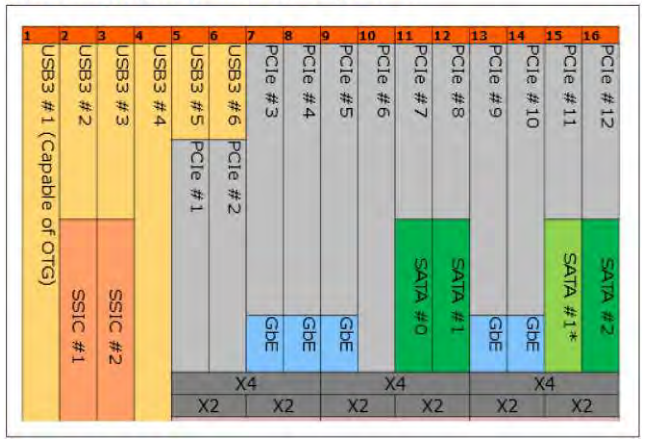


When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

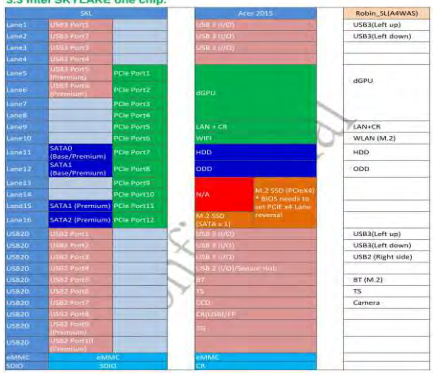
Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA

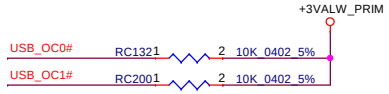
High Speed I/O (HSIO) Lane Multiplexing in SKL U



Acer HSIO def i ne
3.3 Intel SKYLAKE one chip.



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA



DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
•When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
•When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
•The processor provides three SATA general purpose input signals,SATAGP[2:0] for SKL U.
These signals can be configured as interlock switch inputs corresponding to a given SATA port.
•When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
•If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

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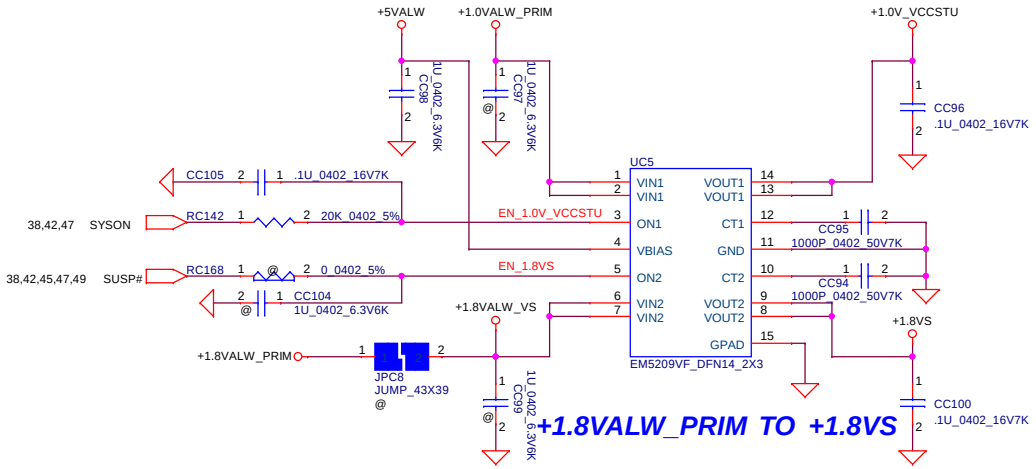
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

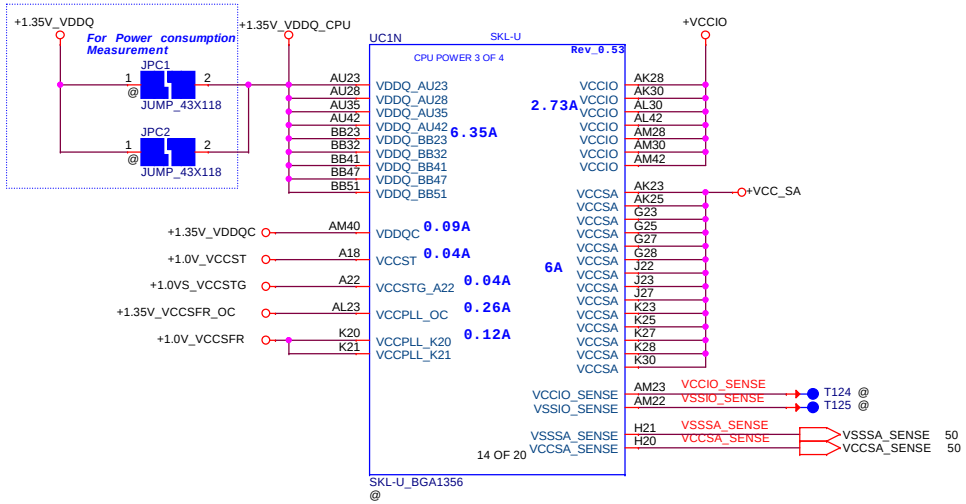
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Thursday, July 16, 2015 | Sheet 12 of 60

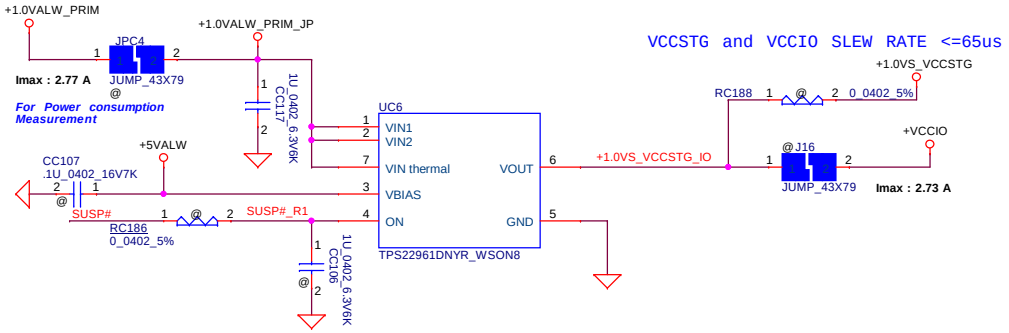
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

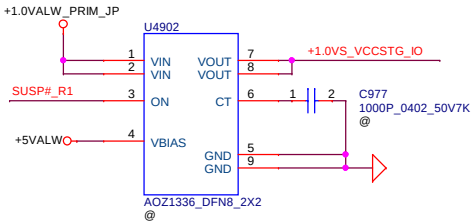


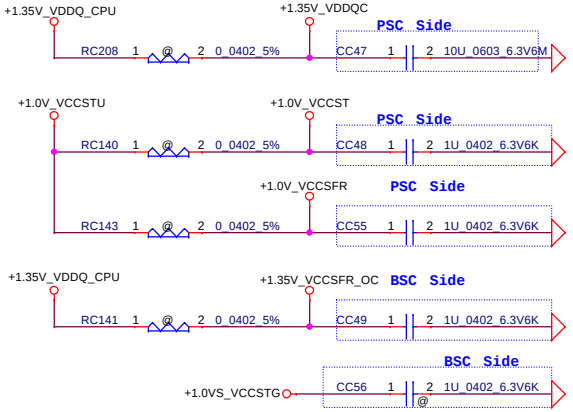
+1.8VALW_PRIM TO +1.8VS



+1.0VALW_PRIM TO +1.0VS_VCCSTG







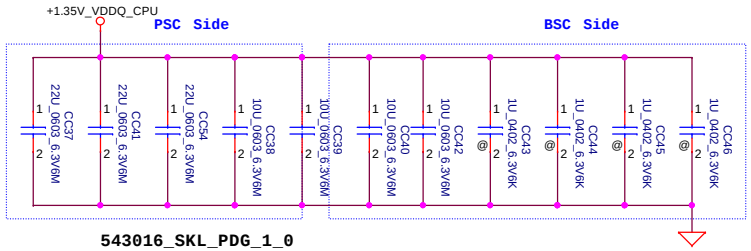
543016_SKL_PDG_1_0
+1.35V_VDDQC : 1x 1uF 0201 (Placeholder)
1x 10uF 0402

543016_SKL_PDG_1_0
+1.0V_VCCST : 1x 1uF 0402

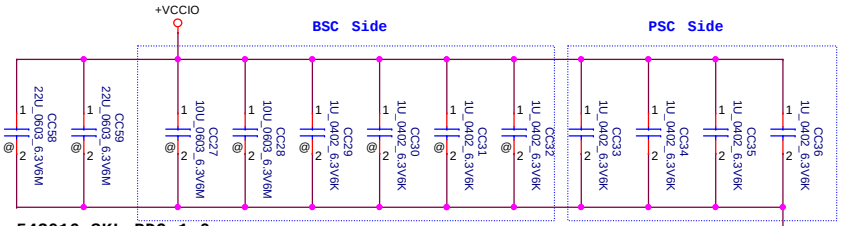
543016_SKL_PDG_1_0
+1.0V_VCCSFR : 1x 1uF 0402

543016_SKL_PDG_1_0
+1.35V_VCCSFR_OC : 1x 1uF 0201

543016_SKL_PDG_1_0
+1.0VS_VCCSTG : 1x 1uF 0402 (Placeholder)



543016_SKL_PDG_1_0
+1.35V_VDDQ_CPU : 2x 10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 10uF 0402
3x 22uF 0603



543016_SKL_PDG_1_0
+VCCIO : 2x10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 1uF 0402

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Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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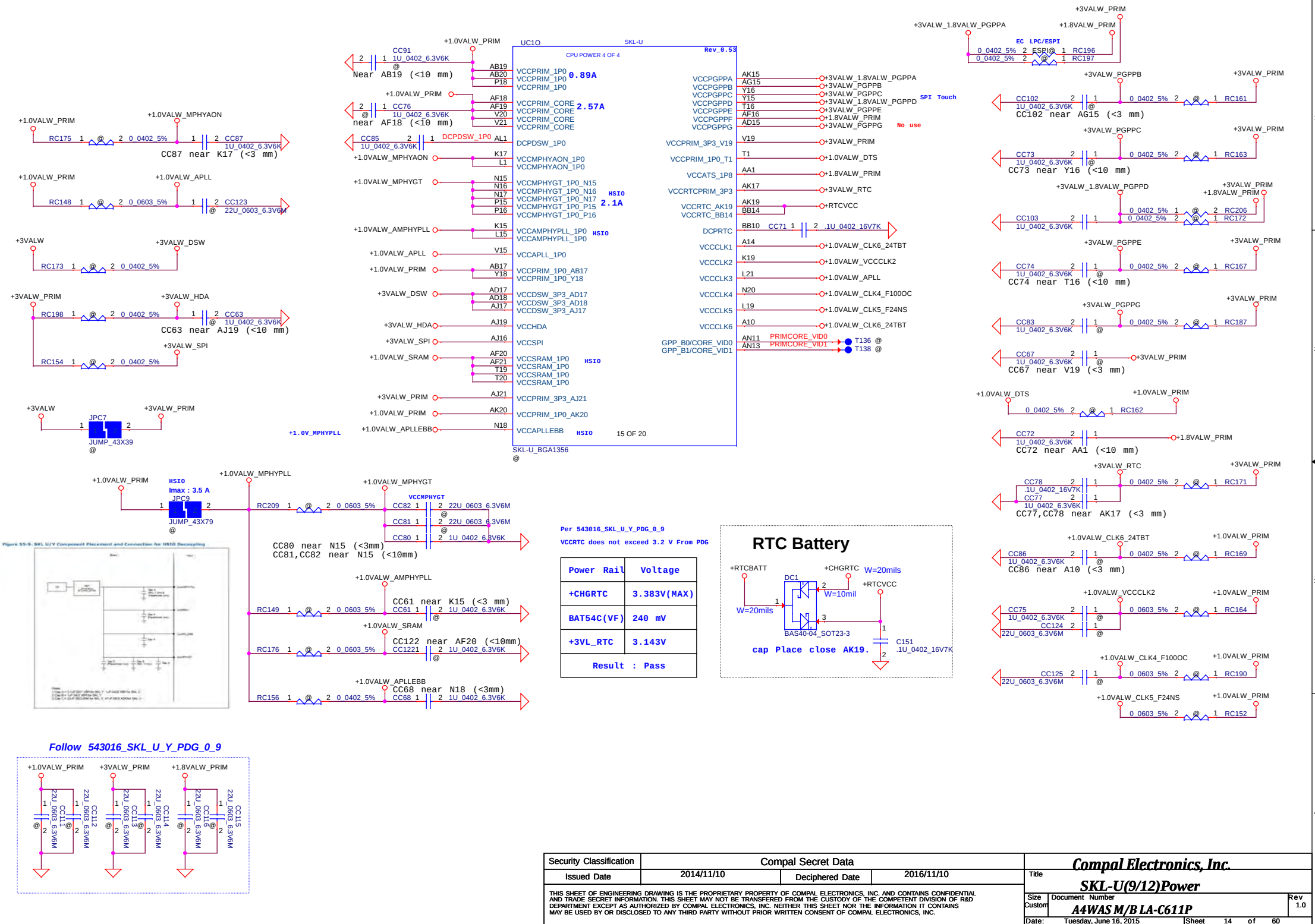

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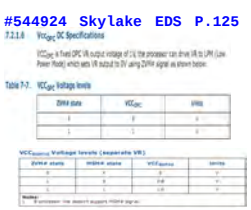
VCC 27A (U 15W Dual Core GT2)

#544924 Skylake EDS P.125



#544924 Skylake EDS P.125
VCCOPC 1V 2.8A
VCC_OPC_1P8 1.8V 50mA
VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

+VCC_CORE

UC1L SKL-U Rev_0.53
CPU POWER 1 OF 4

A30	VCC_A30	VCC_G32	G32
A34	VCC_A34	VCC_G33	G33
A39	VCC_A39	VCC_G35	G35
A44	VCC_A44	VCC_G37	G37
AK33	VCC_AK33	VCC_G38	G38
AK35	VCC_AK35	VCC_G40	G40
AK37	VCC_AK37	VCC_G42	G42
AK38	VCC_AK38	VCC_J30	J30
AK40	VCC_AK40	VCC_J33	J33
AL33	VCC_AL33	VCC_J37	J37
AL37	VCC_AL37	VCC_J40	J40
AL40	VCC_AL40	VCC_K33	K33
AM32	VCC_AM32	VCC_K35	K35
AM33	VCC_AM33	VCC_K37	K37
AM35	VCC_AM35	VCC_K38	K38
AM37	VCC_AM37	VCC_K40	K40
AM38	VCC_AM38	VCC_K42	K42
G30	VCC_G30	VCC_K43	K43
K32	RSVD_K32	VCC_SENSE	E32
AK32	RSVD_AK32	VSS_SENSE	E33
AB62	VCCOPC_AB62	VIDALERT#	B63
P62	VCCOPC_P62	VIDSCK	A63
V62	VCCOPC_V62	VIDSOUT	D64
H63	VCC_OPC_1P8_H63	VCCSTG_G20	G20
G61	VCC_OPC_1P8_G61		
AC63	VCCOPC_SENSE		
AE63	VSSOPC_SENSE		
AE62	VCCEOPIO		
AG62	VCCEOPIO		
AL63	VCCEOPIO_SENSE		
AJ62	VSSEOPIO_SENSE		

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SKL-U_BGA1356
@

T132 @ VCCOPC_SENSE
T133 @ VSSOPC_SENSE
T137 @ VCCEOPIO_SENSE
T139 @ VSSEOPIO_SENSE

+VCC_CORE

#544924 Skylake EDS P.120
VCC U(15W)-dual core GT2 27A(Typ)-33A(MAX)
0.55-1.15V

Trace Length < 25 mils

VCCSENSE 50
VSSSENSE 50
SOC_SVID_ALERT#
SOC_SVID_CLK
SOC_SVID_DAT
SOC_SVID_CLK 50

+1.0VS_VCCSTG
+1.0VS(SUSP#)

Table 2-1. Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
$Vcc_{_SENSE}$ / $Vss_{_SENSE}$	100Ω	50Ω	<25 mils
Vcc_{GT_SENSE} / Vss_{GT_SENSE}			
Vcc_{GTX_SENSE} / Vss_{GTX_SENSE}			
Vcc_{SA_SENSE} / Vss_{SA_SENSE}			
Vcc_{IO_SENSE} / Vss_{IO_SENSE} [1]		NA	

Note: [1] Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/Vss_SENSE lines
- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain a 25-mil separation distance away from any other dynamic signals

VCCGT / VCCGTX(2+3e only) 40A(need confirm)

+VCC_GT

#544924 Skylake EDS P.121
VCCGT U(15W)-dual core GT2 40A(MAX)
0.55-1.15V

UC1M SKL-U Rev_0.53
CPU POWER 2 OF 4

A48	VCCGT	VCCGT	N70
A53	VCCGT	VCCGT	N71
A58	VCCGT	VCCGT	R63
A62	VCCGT	VCCGT	R64
A66	VCCGT	VCCGT	R65
AA63	VCCGT	VCCGT	R66
AA64	VCCGT	VCCGT	R67
AA66	VCCGT	VCCGT	R68
AA67	VCCGT	VCCGT	R69
AA69	VCCGT	VCCGT	R70
AA70	VCCGT	VCCGT	R71
AA71	VCCGT	VCCGT	T62
AC64	VCCGT	VCCGT	U65
AC65	VCCGT	VCCGT	U68
AC66	VCCGT	VCCGT	U71
AC67	VCCGT	VCCGT	W63
AC68	VCCGT	VCCGT	W64
AC69	VCCGT	VCCGT	W65
AC70	VCCGT	VCCGT	W66
AC71	VCCGT	VCCGT	W67
J43	VCCGT	VCCGT	W68
J45	VCCGT	VCCGT	W69
J46	VCCGT	VCCGT	W70
J48	VCCGT	VCCGT	W71
J50	VCCGT	VCCGT	Y62
J52	VCCGT		
J53	VCCGT	VCCGTX_AK42	AK42
J55	VCCGT	VCCGTX_AK43	AK43
J56	VCCGT	VCCGTX_AK45	AK45
J58	VCCGT	VCCGTX_AK46	AK46
J60	VCCGT	VCCGTX_AK48	AK48
K48	VCCGT	VCCGTX_AK50	AK50
K50	VCCGT	VCCGTX_AK52	AK52
K52	VCCGT	VCCGTX_AK53	AK53
K53	VCCGT	VCCGTX_AK55	AK55
K55	VCCGT	VCCGTX_AK56	AK56
K56	VCCGT	VCCGTX_AK58	AK58
K58	VCCGT	VCCGTX_AK60	AK60
K60	VCCGT	VCCGTX_AK70	AK70
L62	VCCGT	VCCGTX_AL43	AL43
L63	VCCGT	VCCGTX_AL46	AL46
L64	VCCGT	VCCGTX_AL50	AL50
L65	VCCGT	VCCGTX_AL53	AL53
L66	VCCGT	VCCGTX_AL56	AL56
L67	VCCGT	VCCGTX_AL60	AL60
L68	VCCGT	VCCGTX_AM48	AM48
L69	VCCGT	VCCGTX_AM50	AM50
L70	VCCGT	VCCGTX_AM52	AM52
L71	VCCGT	VCCGTX_AM53	AM53
M62	VCCGT	VCCGTX_AM56	AM56
N63	VCCGT	VCCGTX_AM58	AM58
N64	VCCGT	VCCGTX_AU58	AU58
N66	VCCGT	VCCGTX_AU63	AU63
N67	VCCGT	VCCGTX_BB57	BB57
N69	VCCGT	VCCGTX_BB66	BB66
J70	VCCGT_SENSE	VCCGTX_SENSE	AK62
J69	VSSGT_SENSE	VSSGTX_SENSE	AL61

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SKL-U_BGA1356
@

50 VCCGT_SENSE
50 VSSGT_SENSE
VCCGT_SENSE
VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE
T155 @
T219 @

Trace Length < 25 mils

For CPU2+3e SKU

SVID ALERT

+1.0V_VCCST

Place the PU resistors close to CPU

RC179
56_0402_5%

SOC_SVID_ALERT#
RC180 1 2 220_0402_5%
SOC_SVID_ALERT#_R 50 (To VR)

SVID DATA

+1.0V_VCCST

Place the PU resistors close to CPU

RC181
100_0402_1%

SOC_SVID_DAT
SOC_SVID_DAT 50 (To VR)

543016 PDG0.9 P.189 Need check

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDSCK							100	100	0	10	
VIDALERT#							56	Empty	220	0	

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Title: SKL-U(10/12)Power,SVID

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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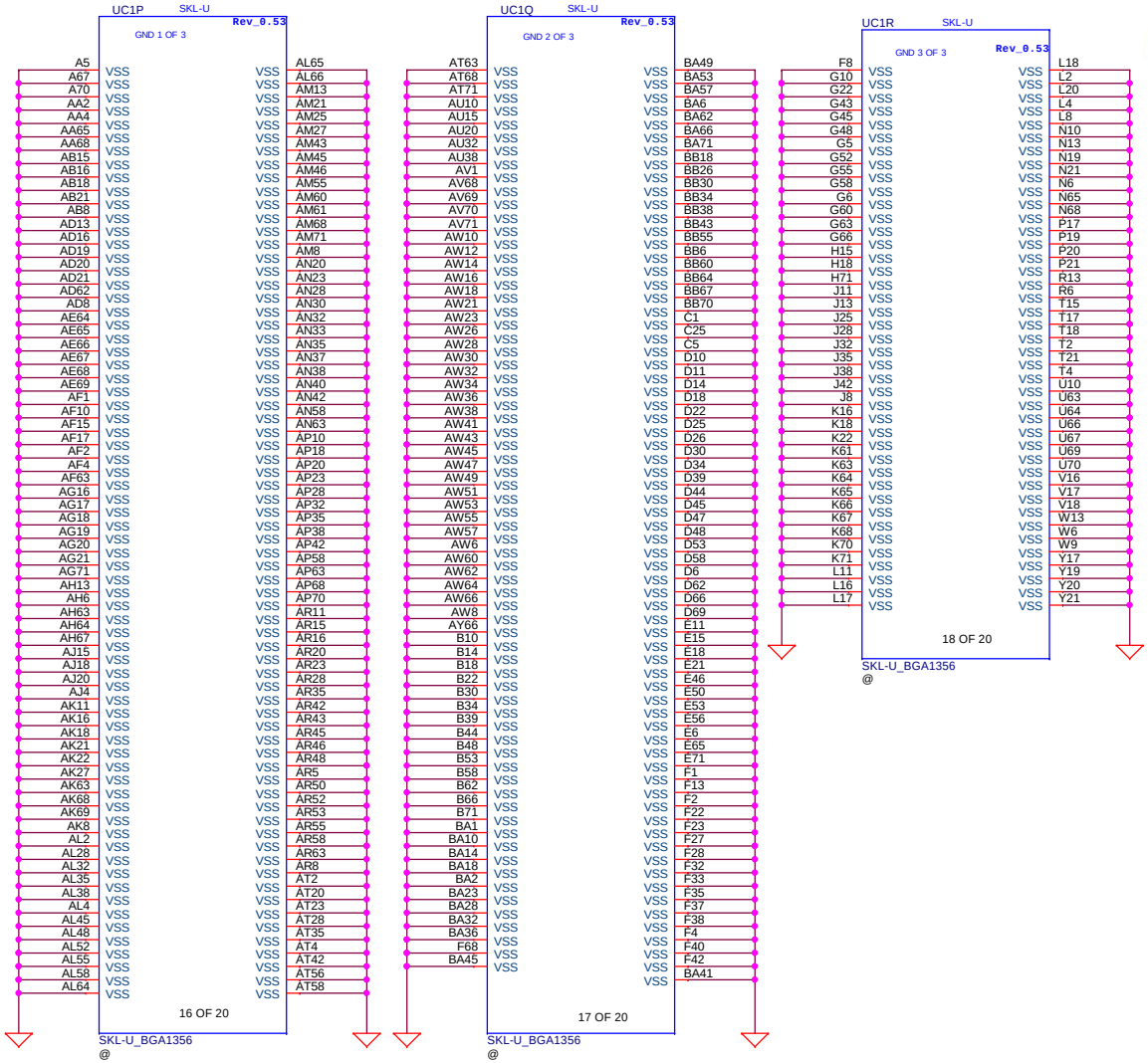
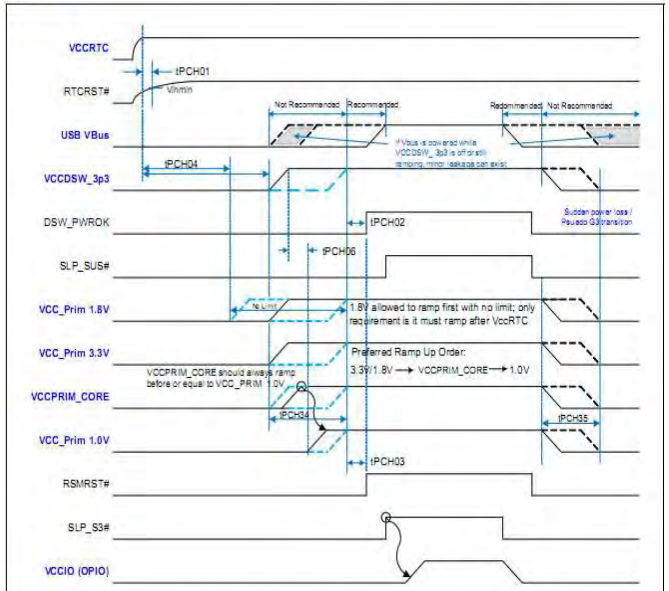


Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



Notes:

1. VCC_PRIM 1.8 V includes VCCPGPPF, VCCATS and may include VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCC_PRIM 3.3 V includes VCCPRIM_3p3 and VCCRTCPRIM_3p3.
3. VCCPRIM_CORE is only applicable on SKL U/Y. For SKL H, the rail is merged with VCCPRIM_1p0.
4. VCC_PRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCSRAM_1p0, VCCMPHYAON_1p0, VCCMPHYGT_1p0, VCCMPHYPLL_1p0, VCCAPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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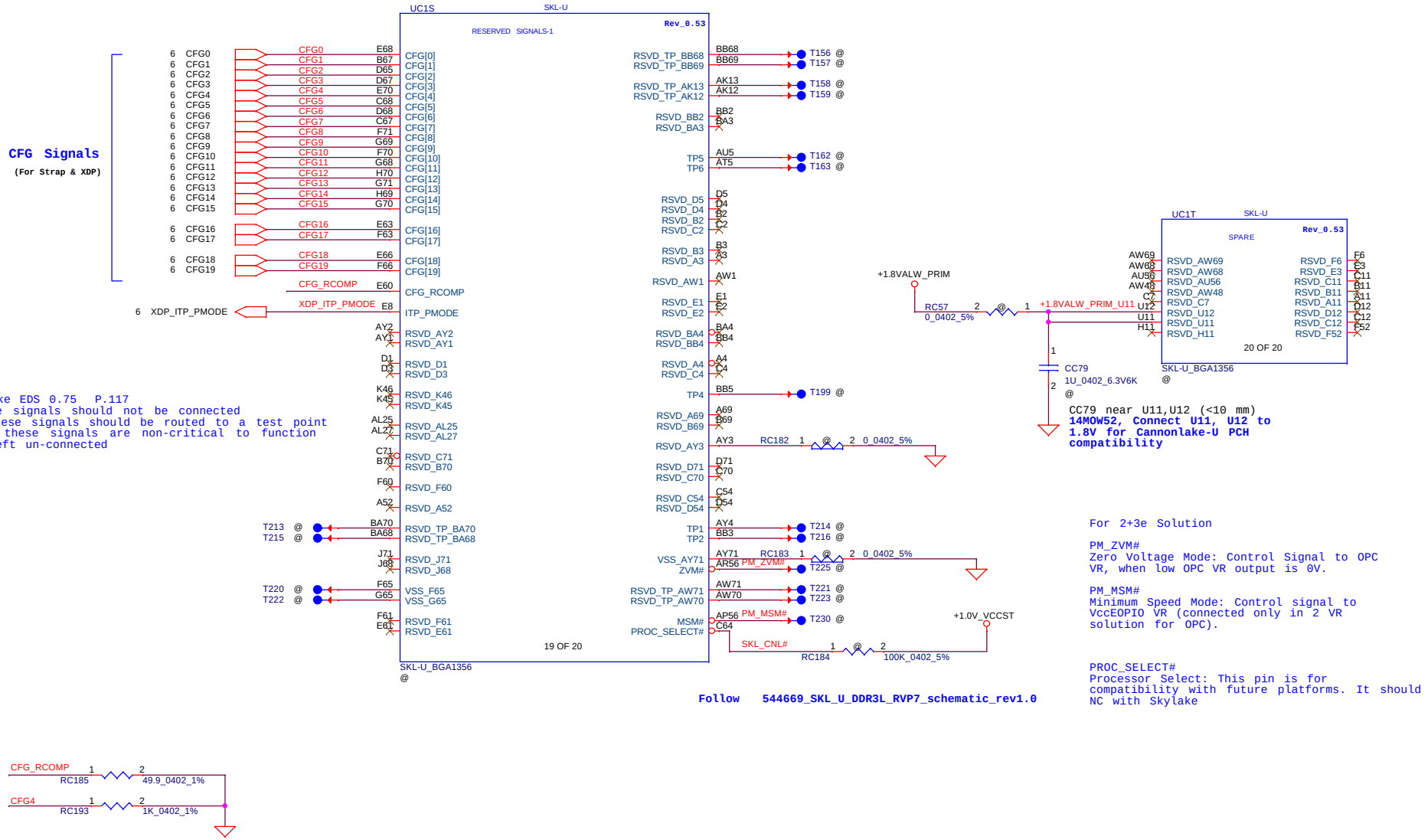
Compal Electronics, Inc.

Title: SKL-U(11/12)GND

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 16 of 60



#544924 SKylake EDS 0.75 P.117
*RSVD - these signals should not be connected
*RSVD_TP - these signals should be routed to a test point
*RSVD_NCTF - these signals are non-critical to function
and may be left un-connected

CC79 near U11,U12 (<10 mm)
14MOW52, Connect U11, U12 to 1.8V for Cannonlake-U PCH compatibility

For 2+3e Solution

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).

PROC_SELECT#
Processor Select: This pin is for compatibility with future platforms. It should NC with Skylake

Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

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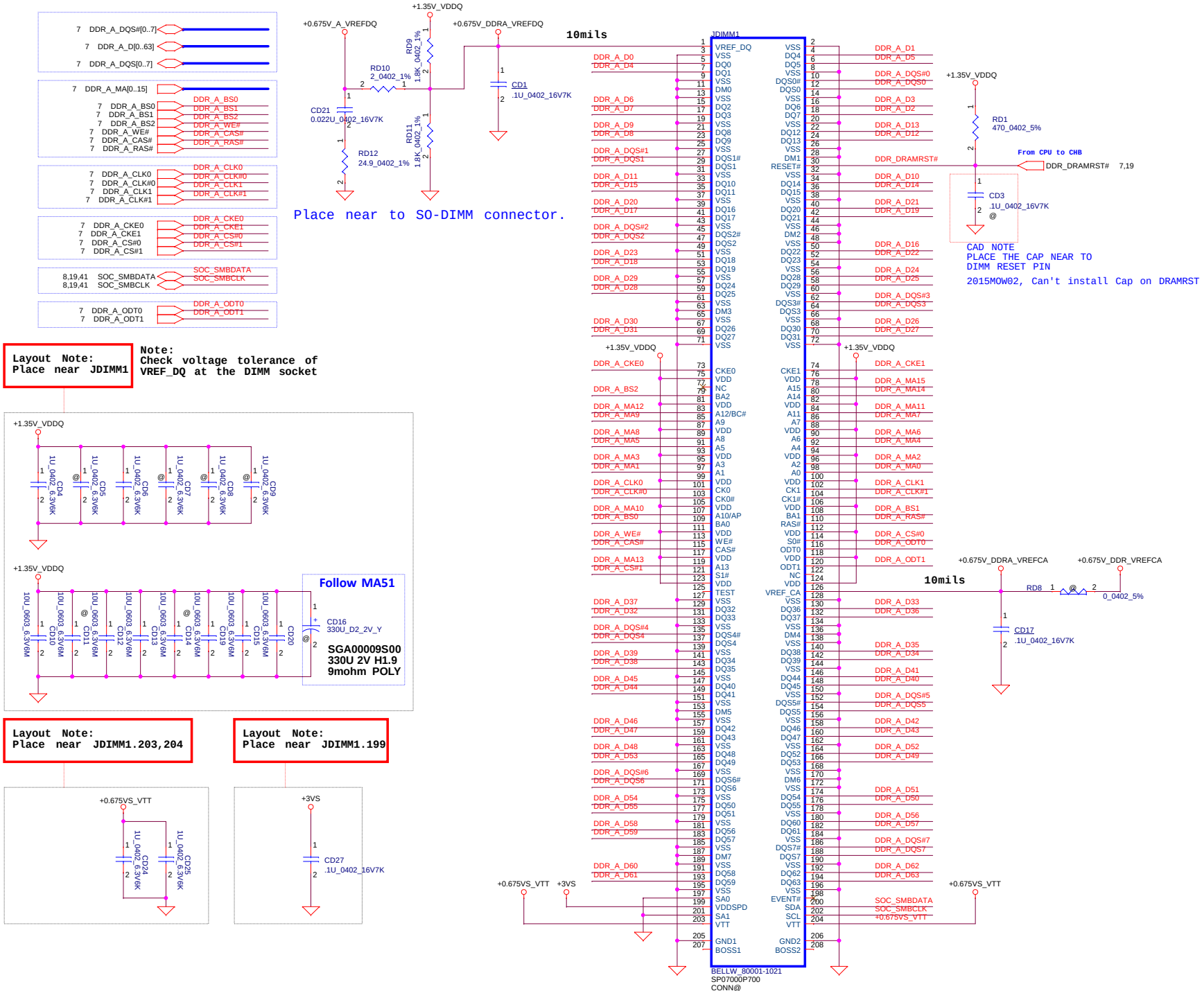
Date: Tuesday, June 16, 2015 | Sheet 17 of 60

Reverse Type

2-3A to 1 DIMMs/channel



Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

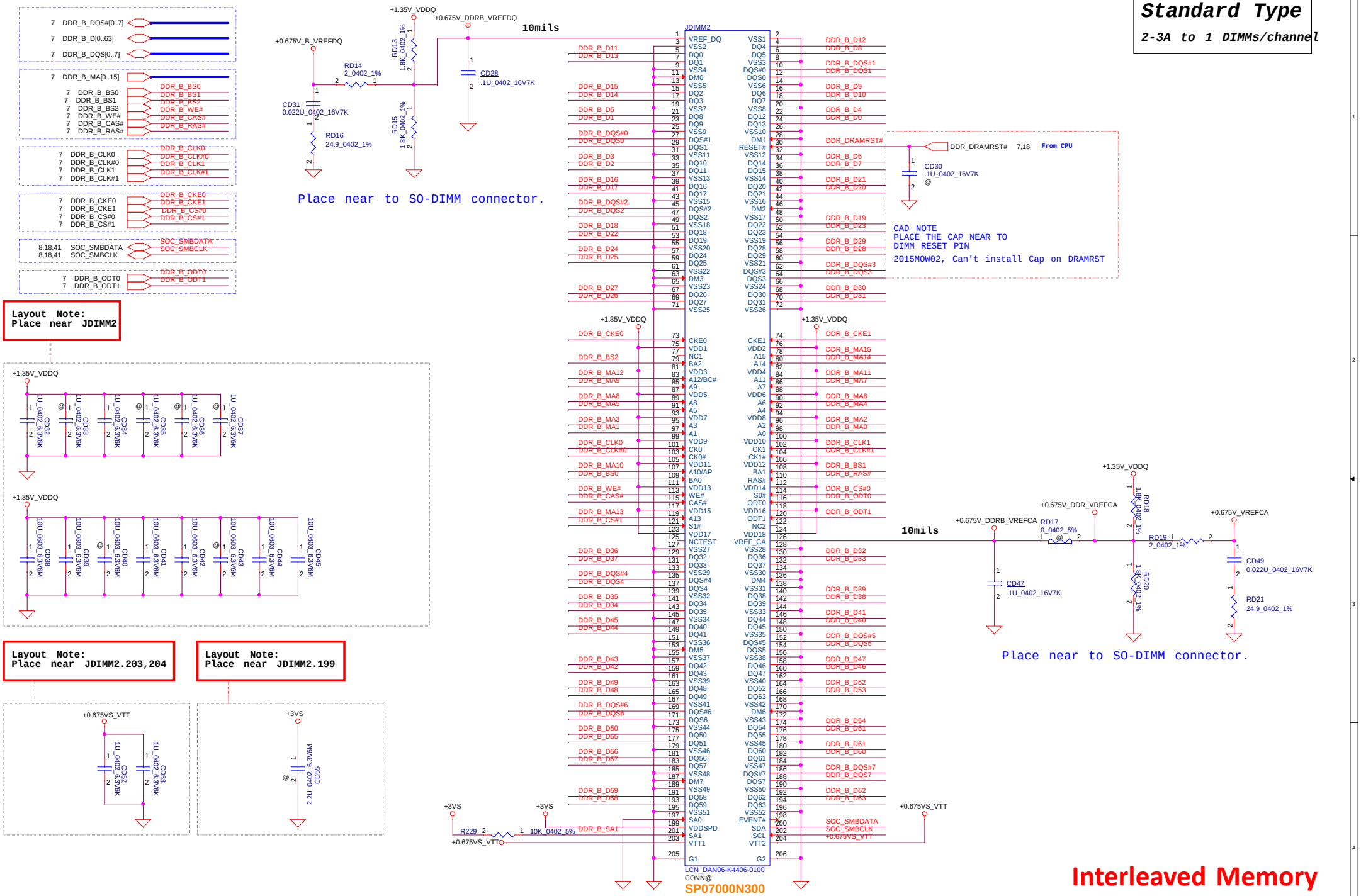
Title: DDR3L DIMMA

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 18 of 60

Standard Type

2-3A to 1 DIMMs/channel



Interleaved Memory

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDR3L DIMMB

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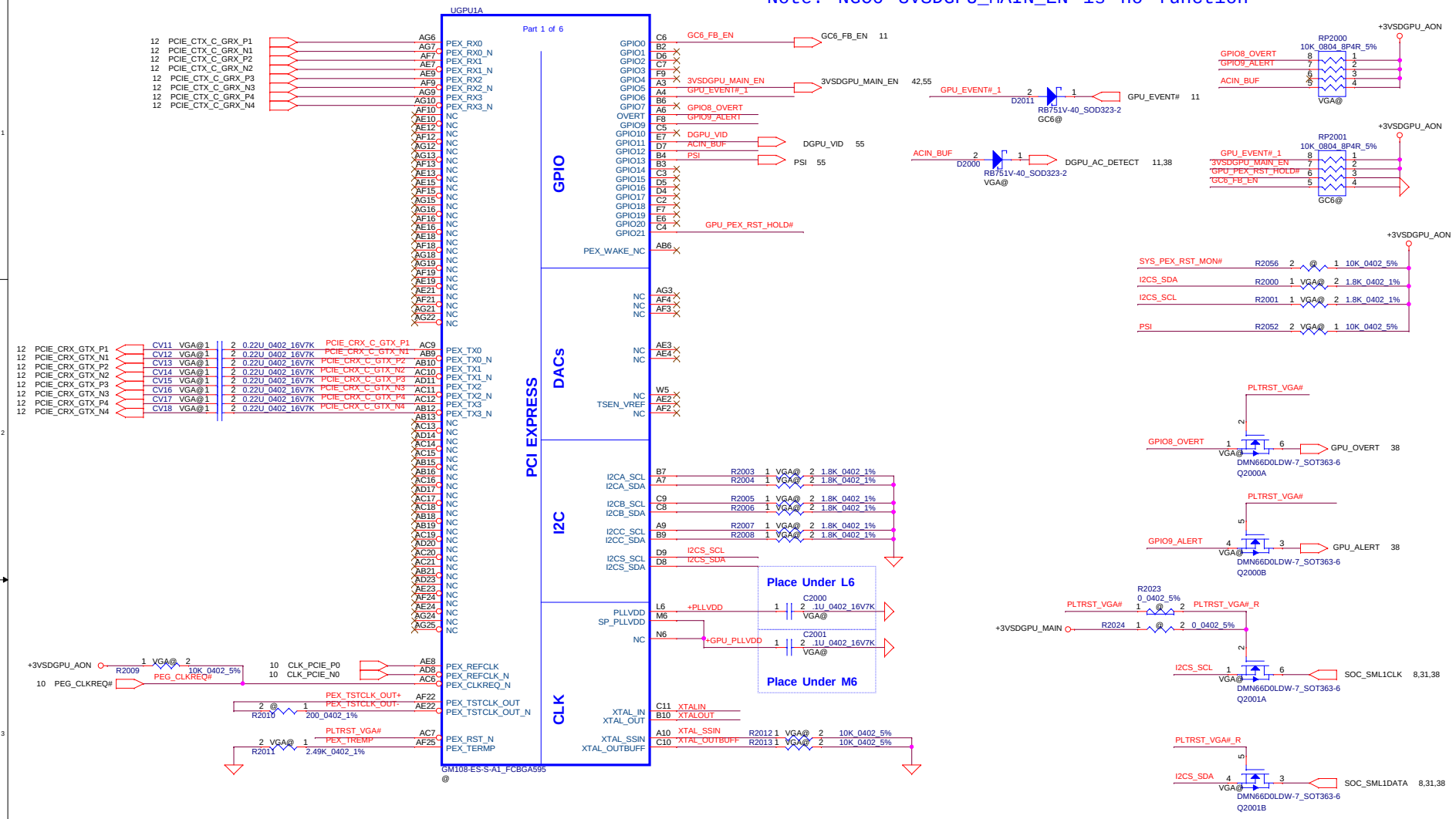
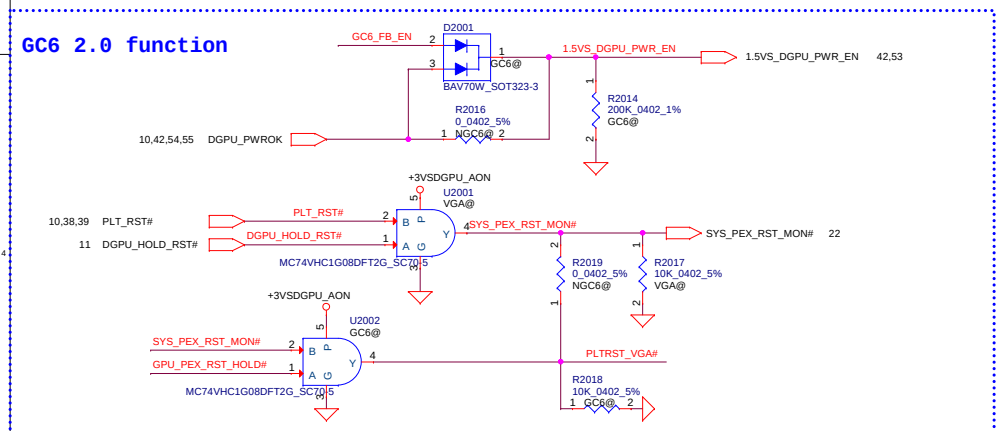
Date: Tuesday, June 16, 2015 | Sheet 19 of 60

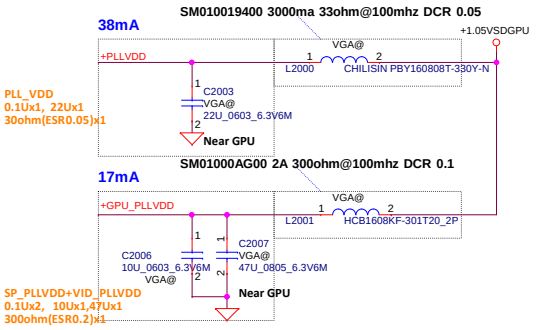
Note: NGC6 3VSDGPU_MAIN_EN is no function

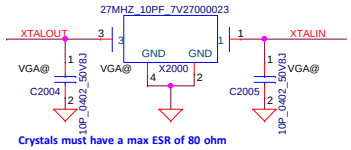


GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

GC6 2.0 function







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Compal Electronics, Inc.

Title: N16X PEG 1/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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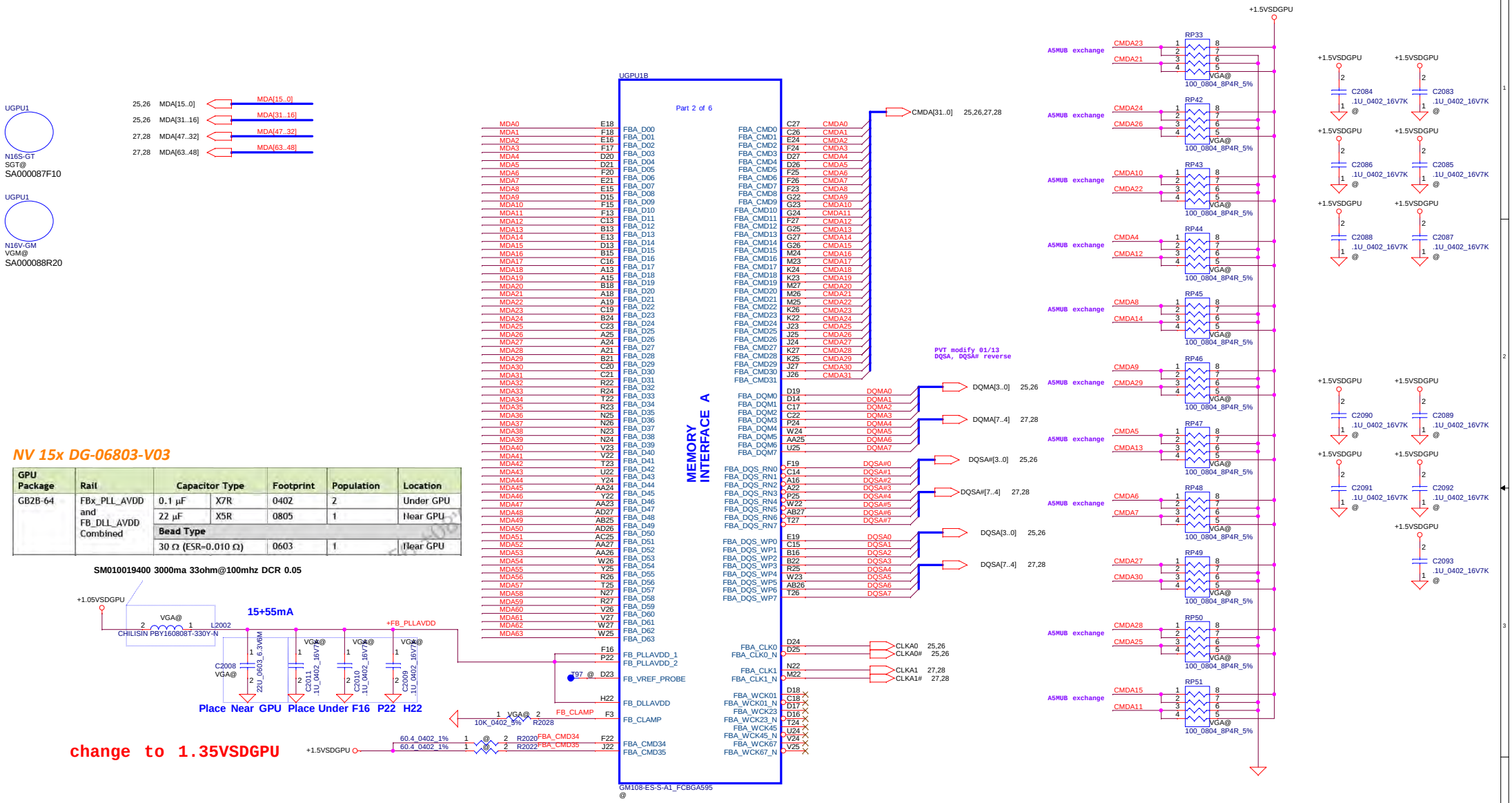
VRAM Interface



NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05

change to 1.35VSDGPU

Security Classification	Compal Secret Data		
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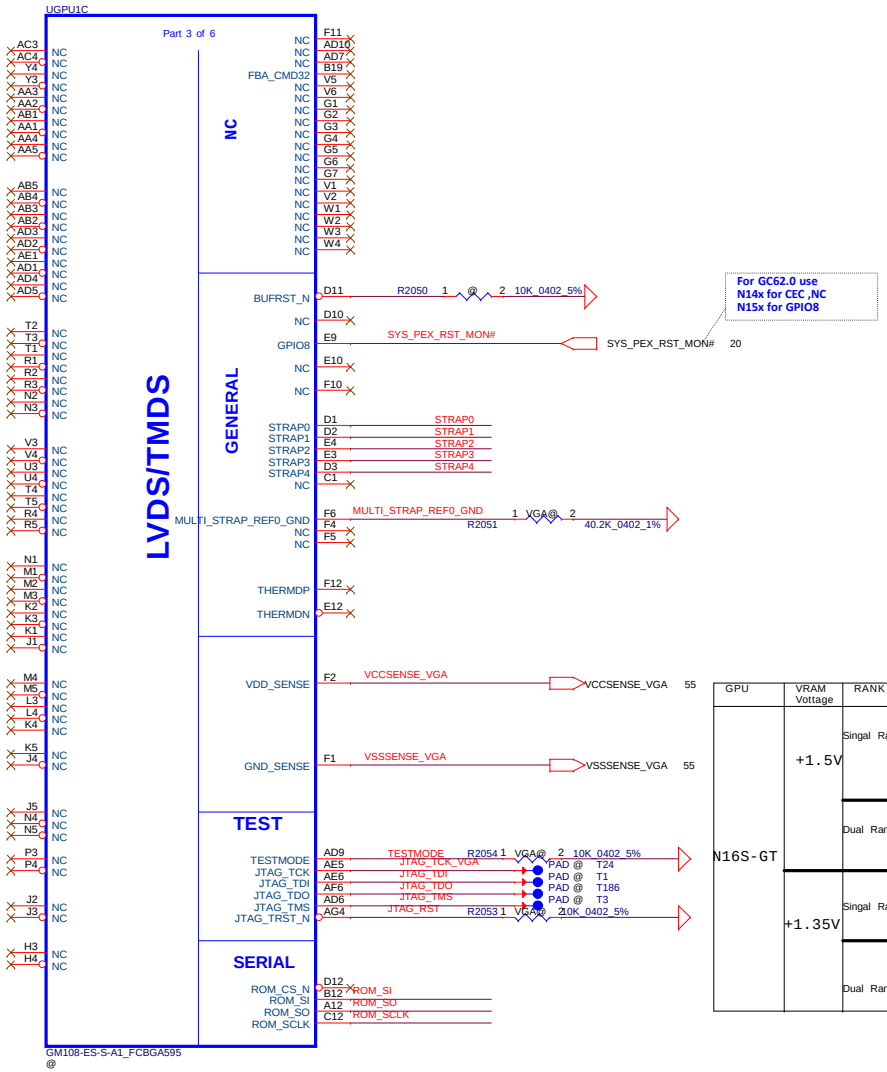
Compal Electronics, Inc.

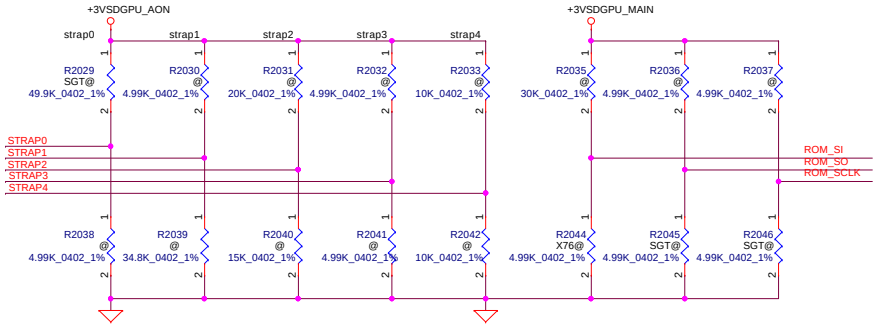
Title: **N16X VRAM 2/9**

Size: Custom | Document Number: **A4WAS M/B LA-C611P** | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 21 of 60



MULTI LEVEL STRAPS



N16VGM Option Component

```
STRAP0  --->  R2029 2 VGM@1 45.3K_0402_1% SD034453280
STRAP1  --->  R2039 2 VGM@1 45.3K_0402_1% SD034453280
STRAP2  --->  R2031 2 VGM@1 10K_0402_1%   SD034100280
STRAP3  --->  R2041 2 VGM@1 4.99K_0402_1% SD034499180
STRAP4  --->  R2042 2 VGM@1 45.3K_0402_1% SD034453280
ROM_SO  --->  R2036 2 VGM@1 4.99K_0402_1% SD034499180
ROM_SCLK--->  R2037 2 VGM@1 4.99K_0402_1% SD034499180

ROM_SI pull down 15kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x2
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x4
ROM_SI pull up 35kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0xE
ROM_SI pull up 30kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0xD
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
ROM_SI pull up 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0xC
```

N16SGT Option Component

```
ROM_SI pull down 4.99kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 15kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x2
ROM_SI pull down 20kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x4
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
```

For N16S-GT Multi strap table

Decive ID : 0x1347

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Singal Rank	X76629B0L07	1GHz	256Mx16x4 2GB	0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 50K	NC	NC	NC	NC	PD 30K	PD 4.99K	PD 4.99K
			X76629B0L08			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629B0L09			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
			X76629B0L14			0x4 (SA000076PB0) Samsung K4W4G1646E-BC1A						PD 24.9K		
		Dual Rank	X76629B0L10	1GHz	256Mx16x8 4GB	0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 24.9K		
			X76629B0L11			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629B0L12			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x2 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 15K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank		900MHz	256Mx16x8 4GB	0xE (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 35K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		

For N16V-GM Multi strap table

Decive ID : 0x1299

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.5V	Singal Rank	X76629B0L01	1GHz	256Mx16x4 2GB	0x9 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 45.3K	PD45.3K	PU 10K	PD 4.99K	PD 45.3K	PU 10K	PU 4.99K	PU 4.99K
			X76629B0L02			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629B0L03			0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 24.9K		
			X76629B0L13			0xA (SA000076PB0) Samsung K4W4G1646E-BC1A						PU 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x0 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 5K		
						0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank	X76629B0L04	900MHz	256Mx16x8 4GB	0xA (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 15K		
			X76629B0L05			0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
			X76629B0L06			0xC (SA000076P20) Samsung K4W4G1646D-BC1A						PU 24.9K		

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Compal Electronics, Inc.

Title: **N16X STRAPS 3/9**

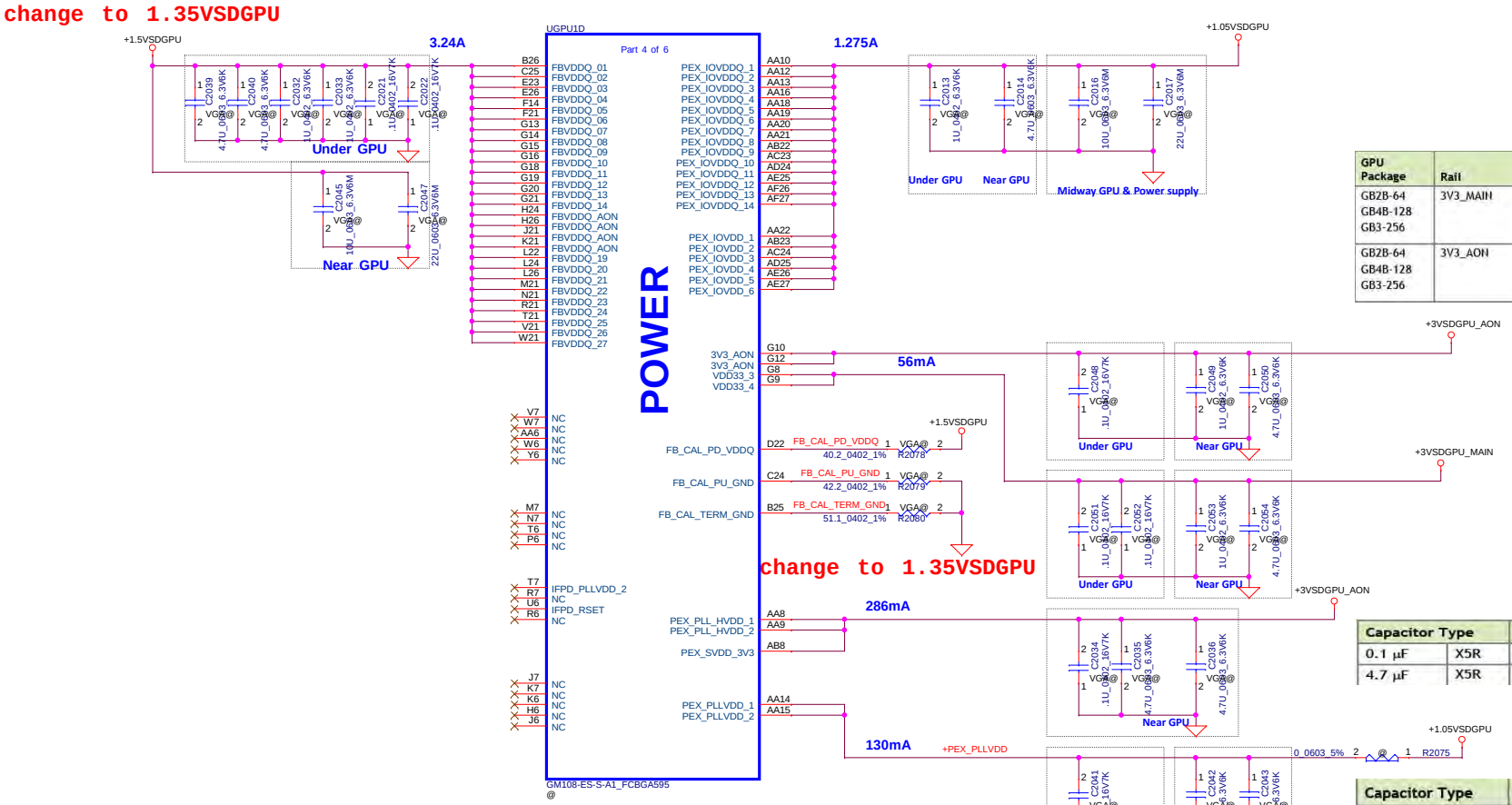
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 22 of 60

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population		Location
GB2B-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 µF	X5R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 µF	X6S	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU

Security Classification: Compal Secret Data
Issued Date: 2014/11/10 Deciphered Date: 2016/11/10

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Compal Electronics, Inc.

Title: N16X POWER & GND 4/9

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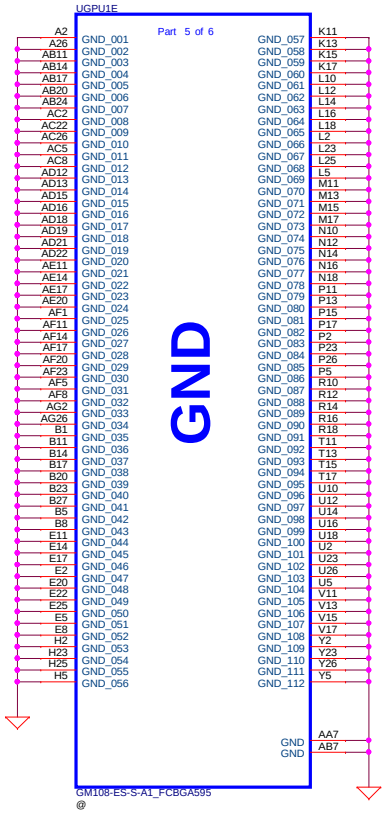

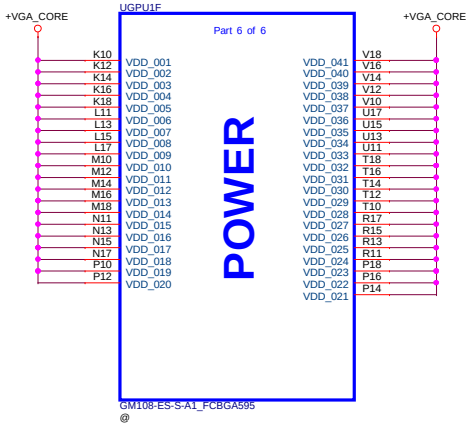

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core — (A)	FB Total 1.5/1.35V (A)	1.05V Total 1.05V (A)
~~N15S-GM~~	~~DDR3/L~~	~~48.11~~	~~4.23~~	~~0.91~~
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102°C

Power Supply Rail (V)	N15V-GM-S DDR3/L (A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102°C

Power Supply Rail (V)	N15V-GL DDR3 (A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: N16X POWER & GND 5/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 24 of 60

VRAM DDR3 chips

21,26,27,28 DQSA[7..0] — DQSA[7..0]
21,26,27,28 DQSA#[7..0] — DQSA#[7..0]
21,26,27,28 DQMA[7..0] — DQMA[7..0]
21,26,27,28 MDA[63..0] — MDA[63..0]
21,26,27,28 CMDA[30..0] — CMDA[30..0]

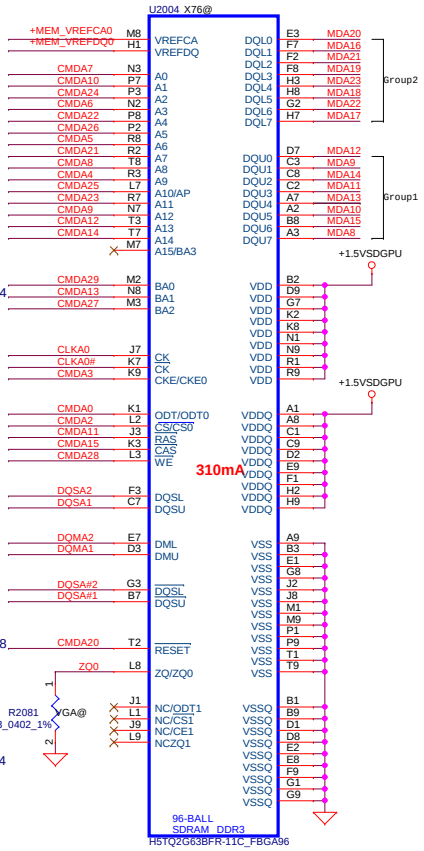
Lower Rank 0 BOT SIDE

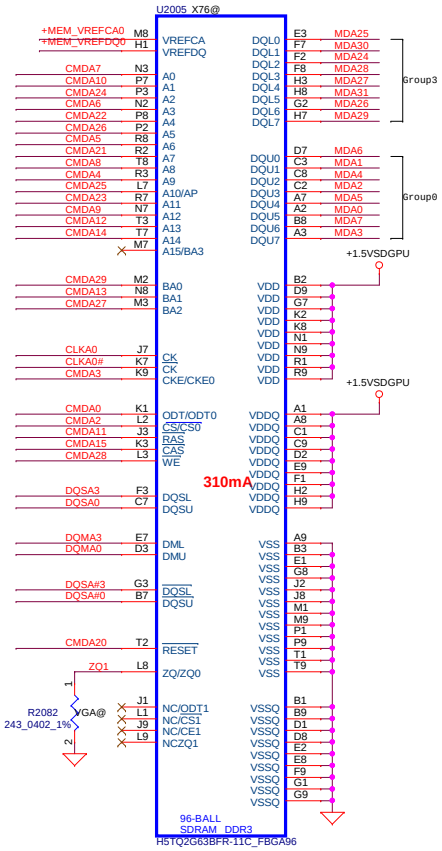
X76 for VGM

ZZZ X7601@ — X76629BOL01 2Gb Hynix 256Mx16x4
ZZZ X7602@ — X76629BOL02 2Gb Micron 256Mx16x4
ZZZ X7603@ — X76629BOL03 2Gb Samsung-D 256Mx16x4
ZZZ X7604@ — X76629BOL04 4Gb Hynix 256Mx16x8
ZZZ X7605@ — X76629BOL05 4Gb Micron 256Mx16x8
ZZZ X7606@ — X76629BOL06 4Gb Samsung-D 256Mx16x8
ZZZ X7613@ — X76629BOL13 2Gb Samsung-E 256Mx16x4

X76 for SGT

ZZZ X7607@ — X76629BOL07 2Gb Hynix 256Mx16x4
ZZZ X7608@ — X76629BOL08 2Gb Micron 256Mx16x4
ZZZ X7609@ — X76629BOL09 2Gb Samsung-D 256Mx16x4
ZZZ X7610@ — X76629BOL10 4Gb Hynix 256Mx16x8
ZZZ X7611@ — X76629BOL11 4Gb Micron 256Mx16x8
ZZZ X7612@ — X76629BOL12 4Gb Samsung-D 256Mx16x8
ZZZ X7614@ — X76629BOL14 2Gb Samsung-E 256Mx16x4



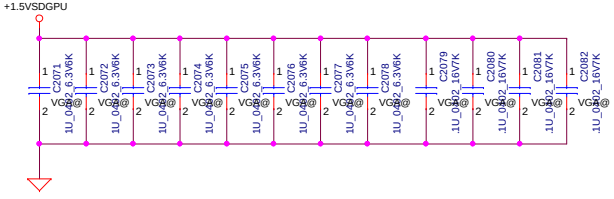


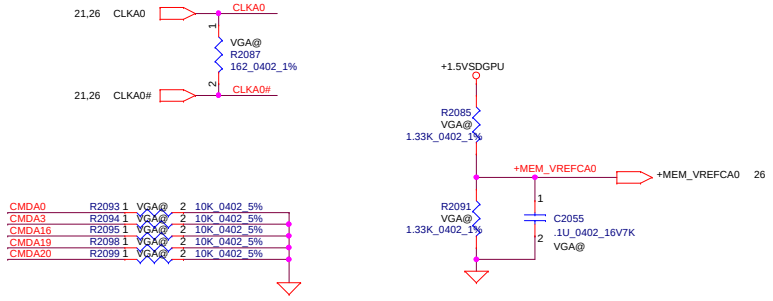
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM





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Title: N16X Upper Rank0 6/9

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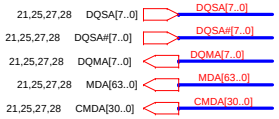
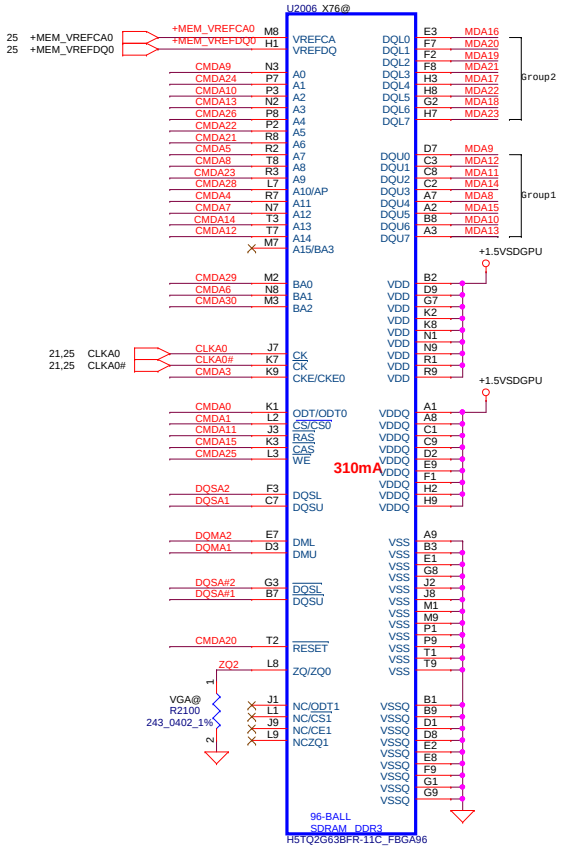
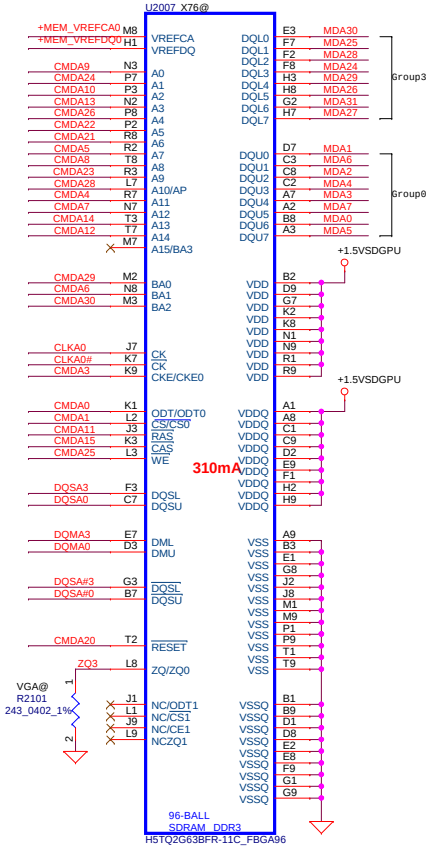
Date: Tuesday, June 16, 2015 | Sheet 25 of 60

VRAM DDR3 chips



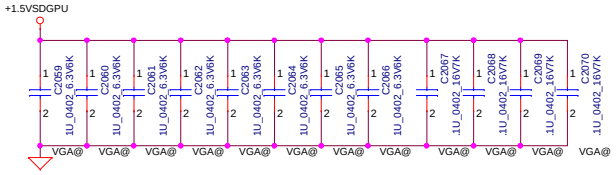
Lower Rank 1 TOP SIDE





Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



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Title: N16X Upper Rank1 7/9

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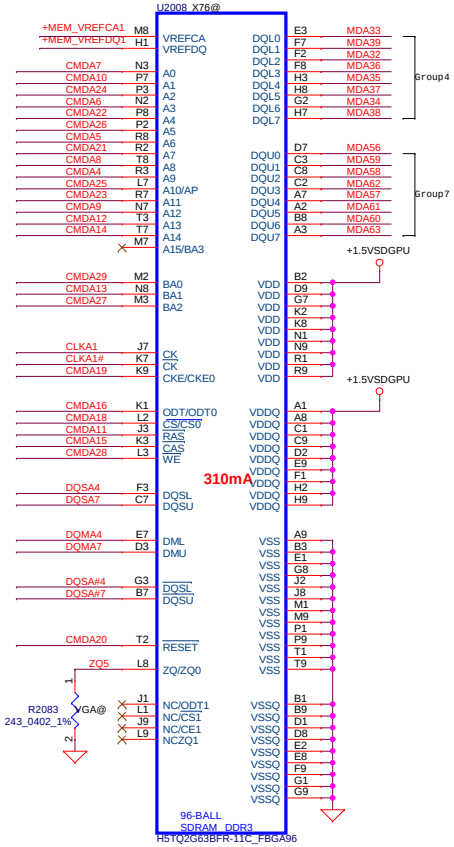
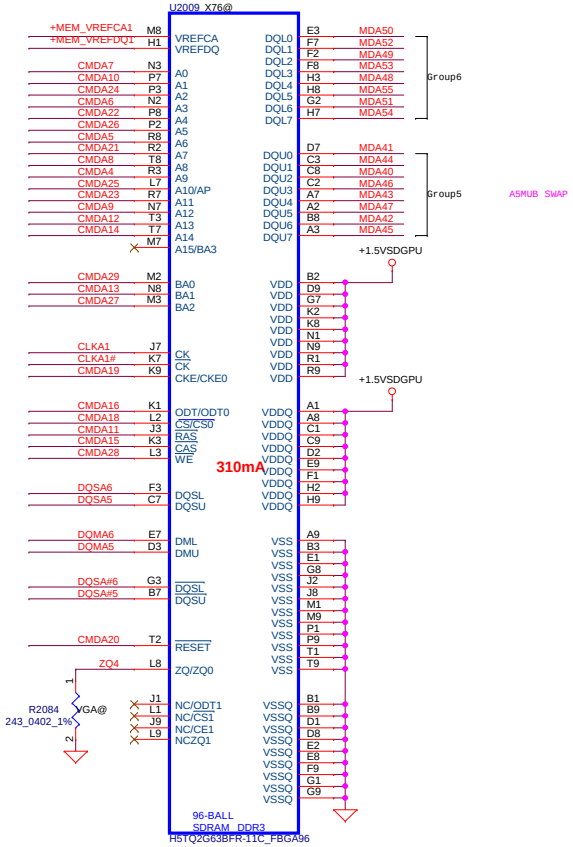
Date: Tuesday, June 16, 2015 | Sheet 26 of 60

VRAM DDR3 chips

21,25,26,28 DQSA[7..0] — DQSA[7..0]
21,25,26,28 DQSA#[7..0] — DQSA#[7..0]
21,25,26,28 DQMA[7..0] — DQMA[7..0]
21,25,26,28 MDA[63..0] — MDA[63..0]
21,25,26,28 CMDA[30..0] — CMDA[30..0]

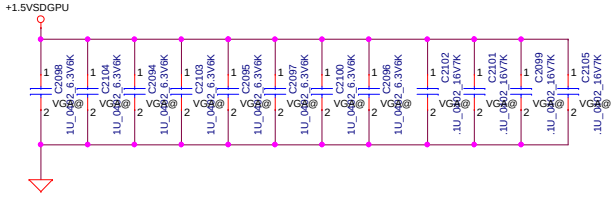
Upper Rank 0 BOT SIDE

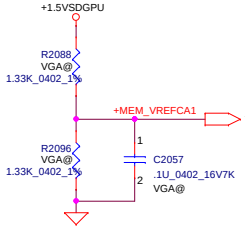


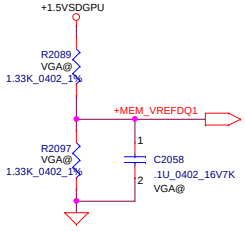


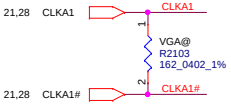
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









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Title: N16X Lower Rank0 8/9

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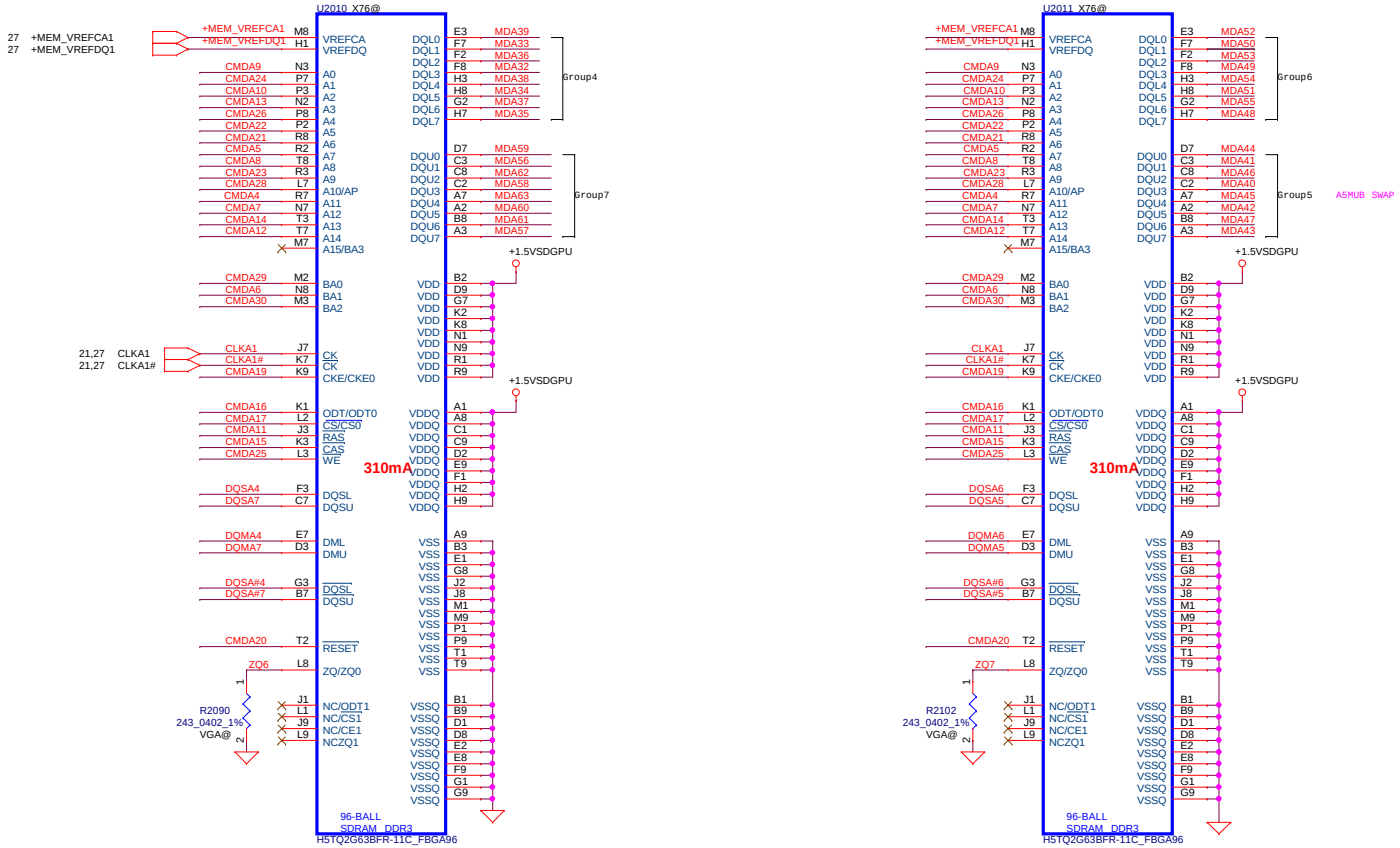
VRAM DDR3 chips

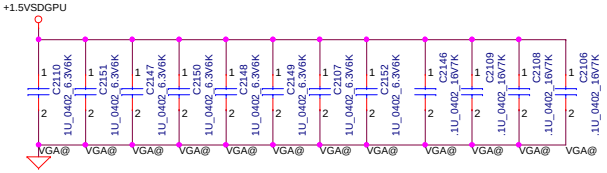
21,25,26,27 DQSA[7..0] — DQSA[7..0]
21,25,26,27 DQSA#[7..0] — DQSA#[7..0]
21,25,26,27 DQMA[7..0] — DQMA[7..0]
21,25,26,27 MDA[63..0] — MDA[63..0]
21,25,26,27 CMDA[30..0] — CMDA[30..0]

Upper Rank 1 TOP SIDE



Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



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Title: N16X Lower Rank1 9/9

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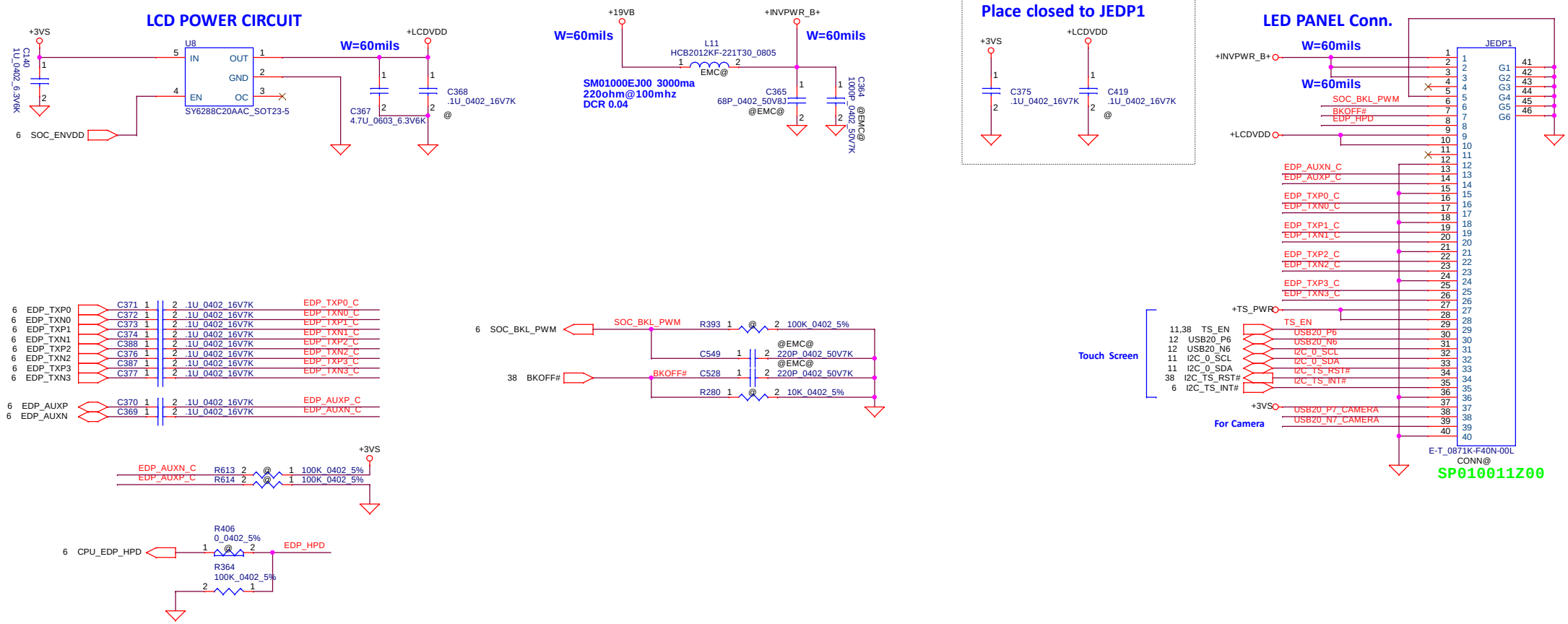
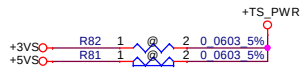
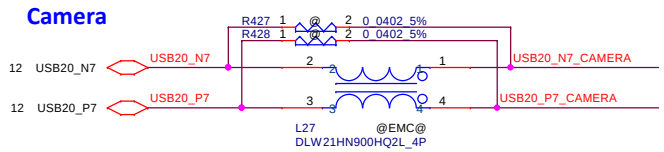
Date: Tuesday, June 16, 2015 | Sheet 28 of 60



I2C Touch Screen



Camera



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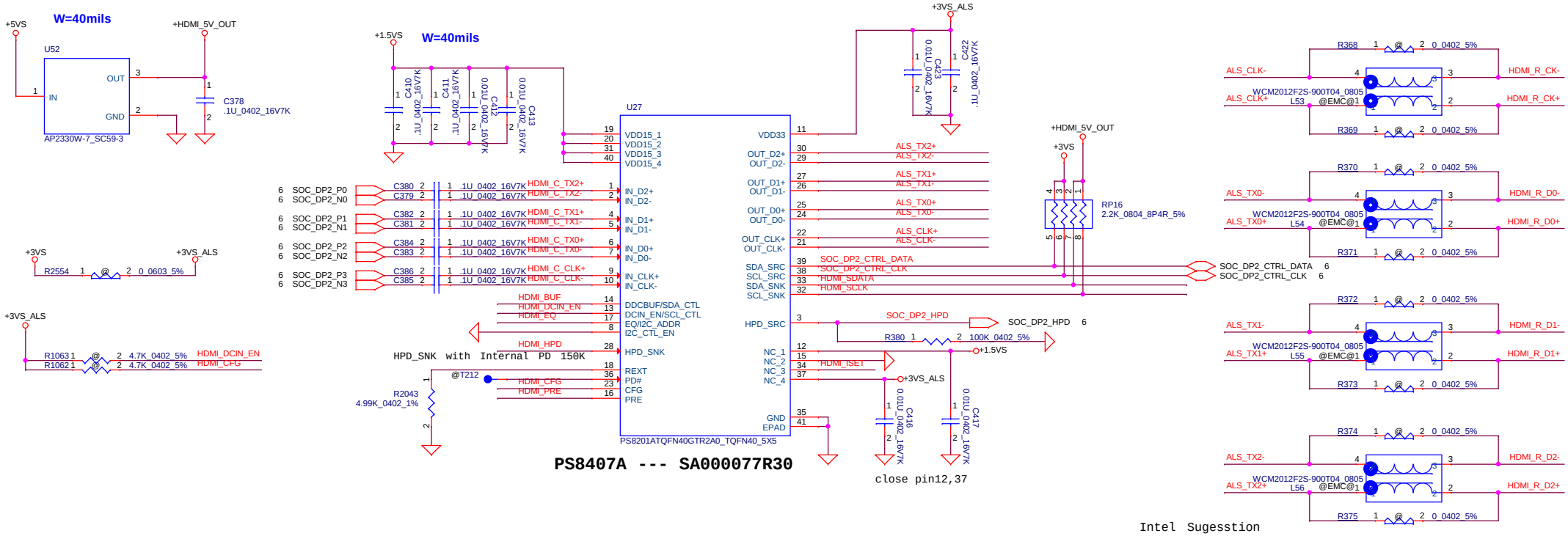
Compal Electronics, Inc.

Title: **eDP Connector**

Size: Custom | Document Number: **A4WAS M/B LA-C611P** | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 29 of 60



PS8407A --- SA000077R30

Enable active DDC buffer;
Internal pull down at ~150KΩ , 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with internal pull up2.36K resistor
M: active DDC buffer without internal pull up resistor

Output pre-emphasis setting;
Internal pull down at ~150kΩ , 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 3.0dB pre-emphasis

Receiver equalization setting;
Internal pull down at ~150kΩ , 3.3V I/O.
L: programmable EQ for channel loss up to 5.3dB
H: programmable EQ for channel loss up to 10dB
M: programmable EQ for channel loss up to 14dB

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/11/10	Deciphered Date	2016/11/10	Title: HDMI CONN.
				Size: Custom; Document Number: A4WAS M/B LA-C611P; Rev: 1.0
				Date: Tuesday, June 16, 2015; Sheet 30 of 60

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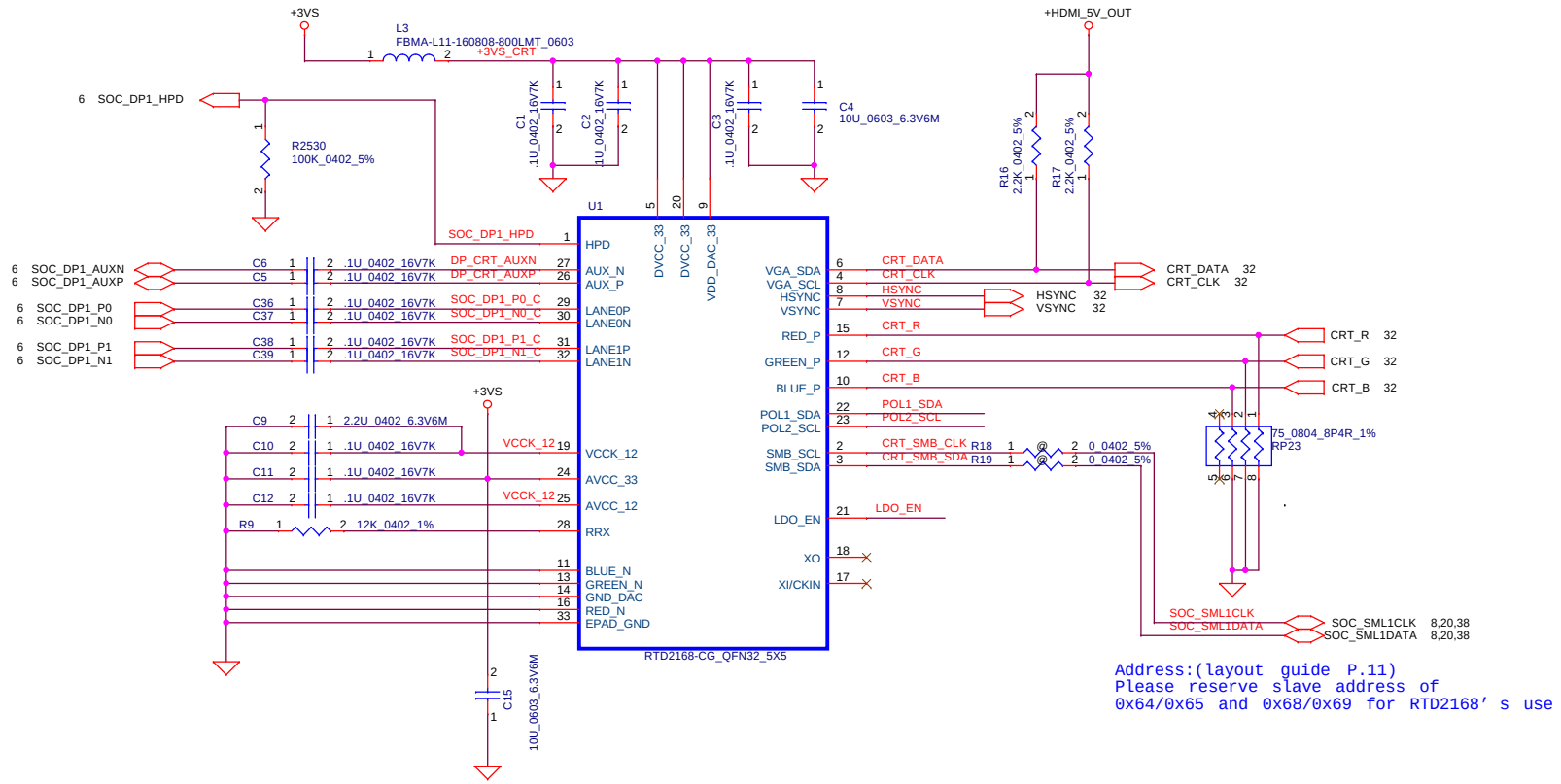

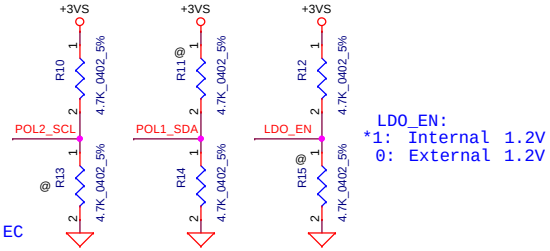

		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM

LDO_EN:
*1: Internal 1.2V
0: External 1.2V

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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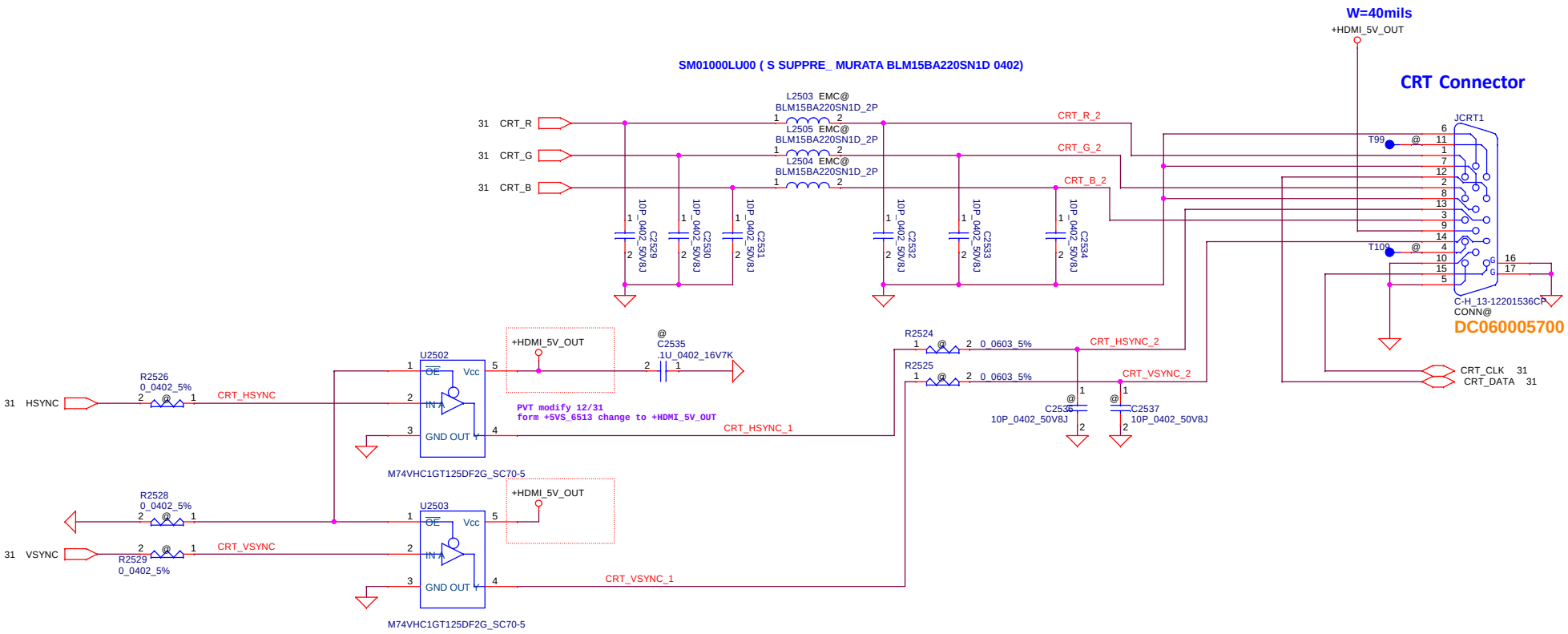
Compal Electronics, Inc.

Title: **Realtek RTD2168**

Size: Custom | Document Number: **A4WAS M/B LA-C611P** | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 31 of 60

CRT conn.



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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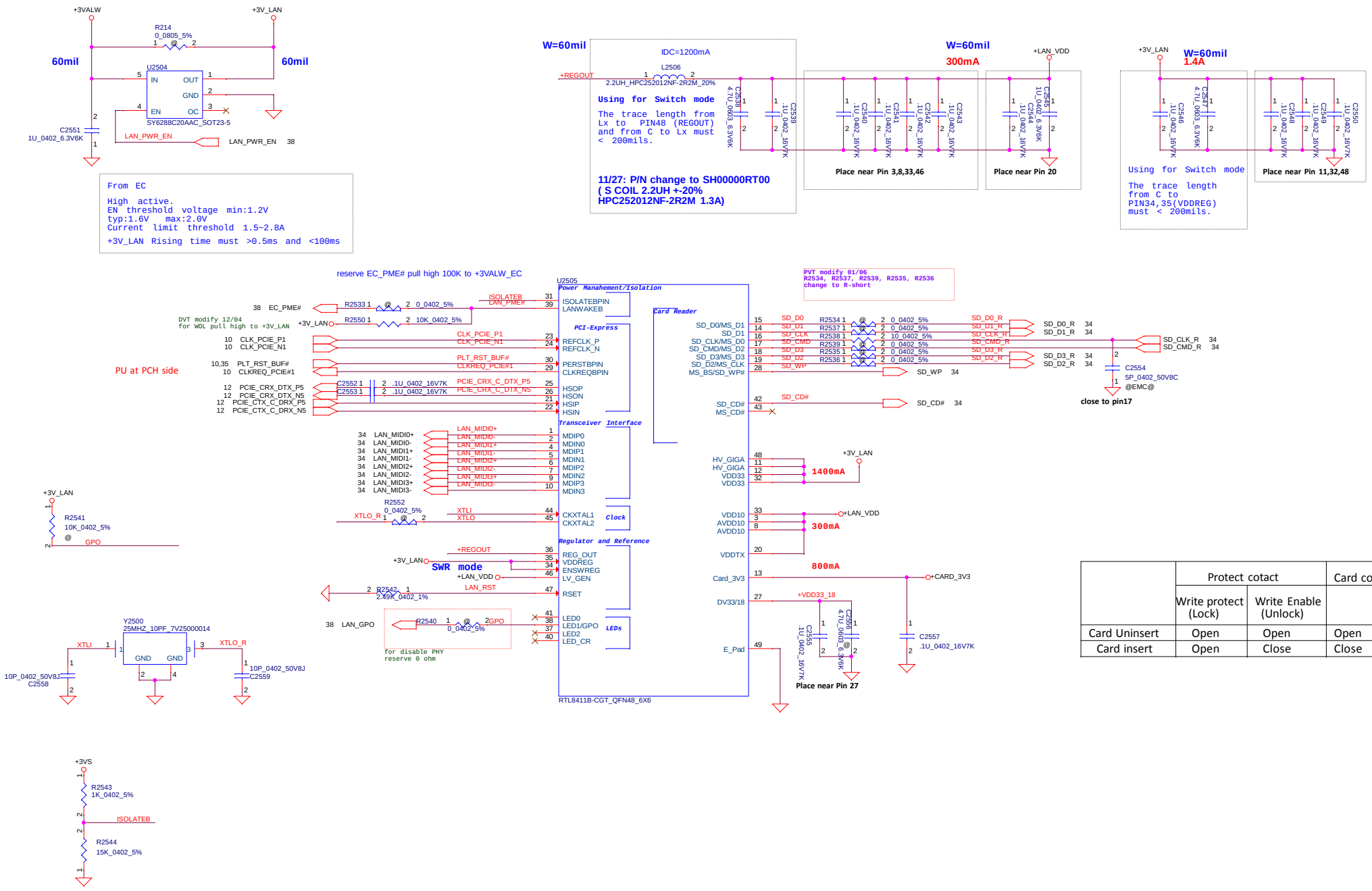
Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **A4WAS M/B LA-C611P** | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 32 of 60

LAN-RTL8411B



	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: LAN RTL8411B

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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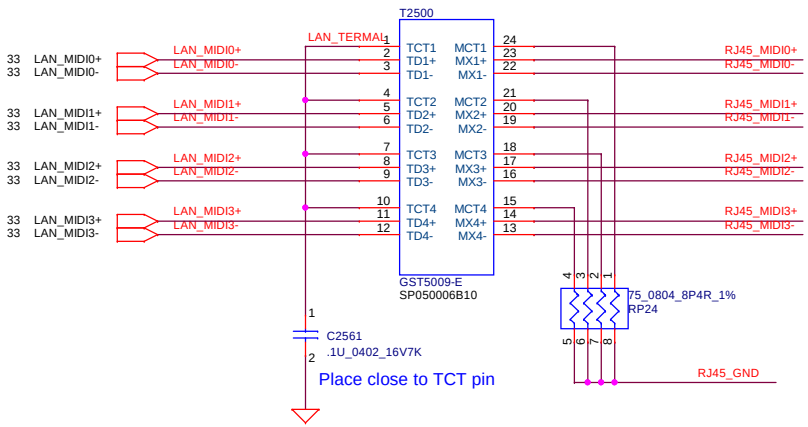
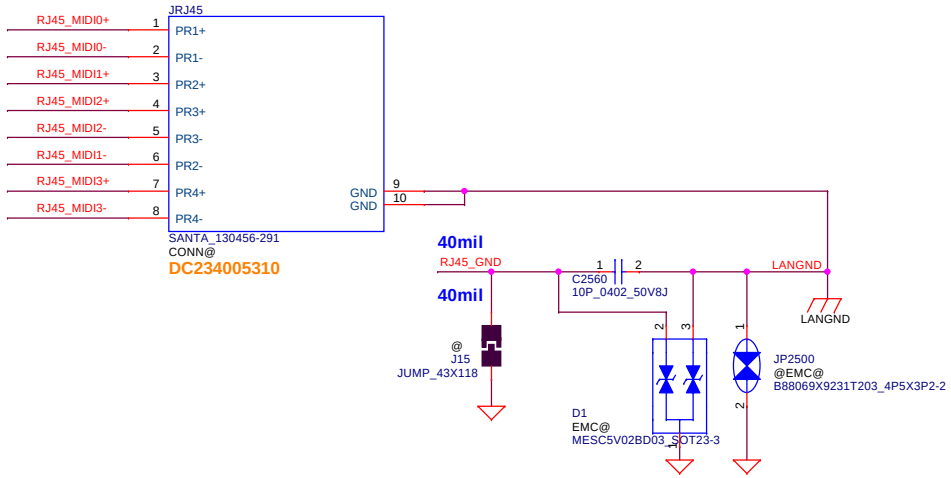
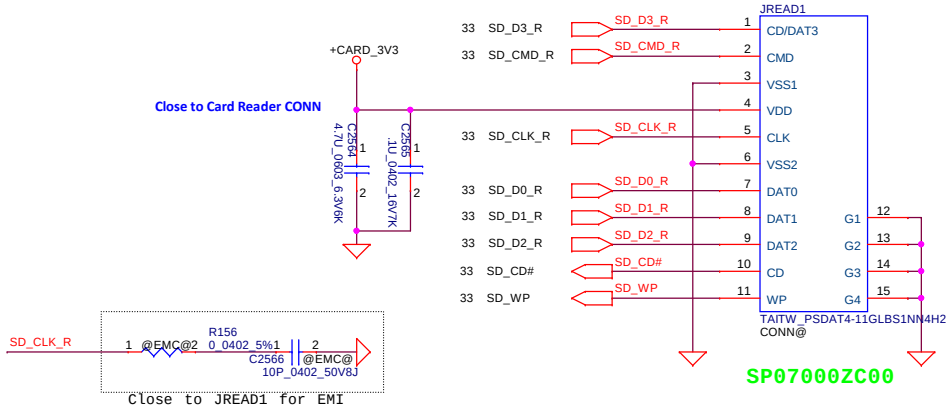
LAN Connector





Card Reader Connector



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Issued Date	2014/11/10	Deciphered Date	2016/11/10	Title: LAN RJ45/CR SD Connector
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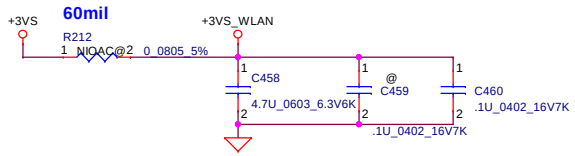
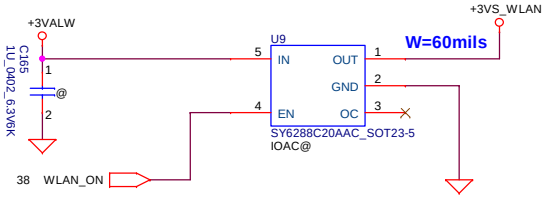
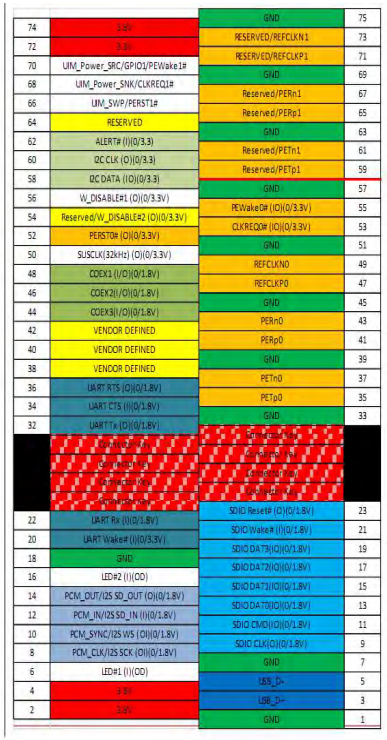
				Date: Tuesday, June 16, 2015; Sheet 34 of 60

Wireless LAN

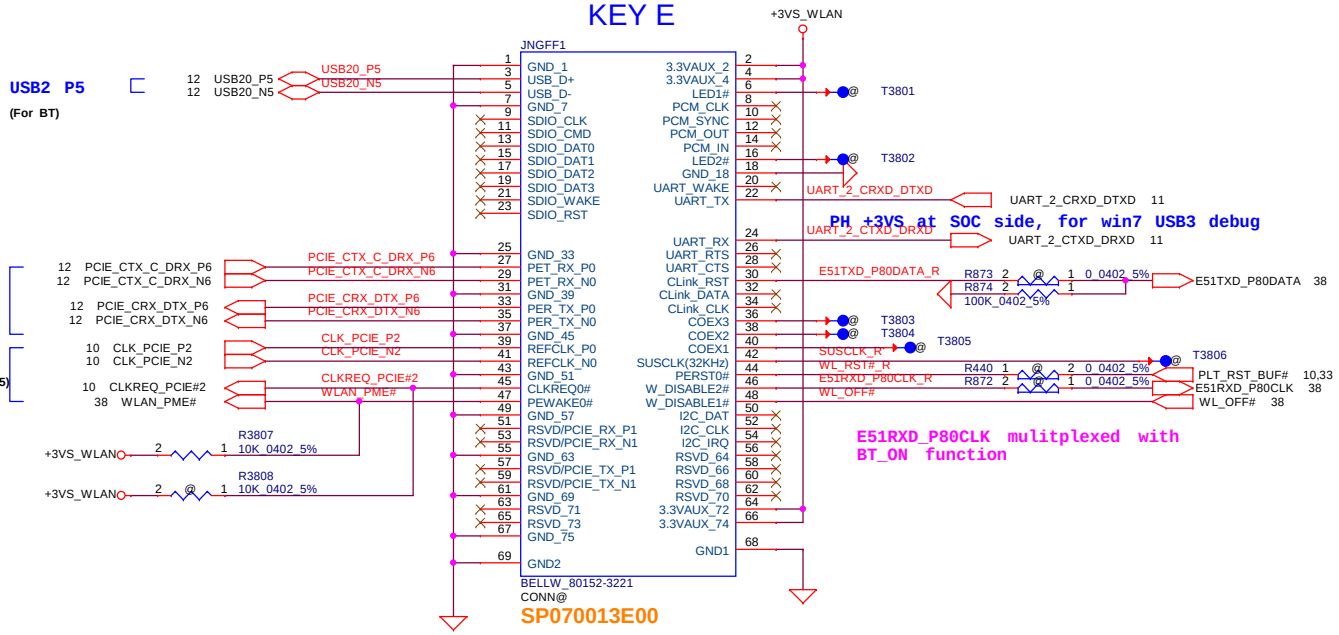




NGFF WL+BT (KEY E)



KEY E



~~3.1.8.1.~~3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~RDX~~ UART_RXD (Input): Receive Data
- ~~RTX~~ UART_TXD (Output): Transmit Data
- UART RTS (Input): Request to Send (Host Flow Control)
- UART CTS (Output): Clear to Send (Device Flow Control)
- ~~Host Wake Up~~UART_Wake# (Output): Host wake-up line is optional in case the host support in band wake-up

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				Date: Tuesday, June 16, 2015; Sheet 35 of 60

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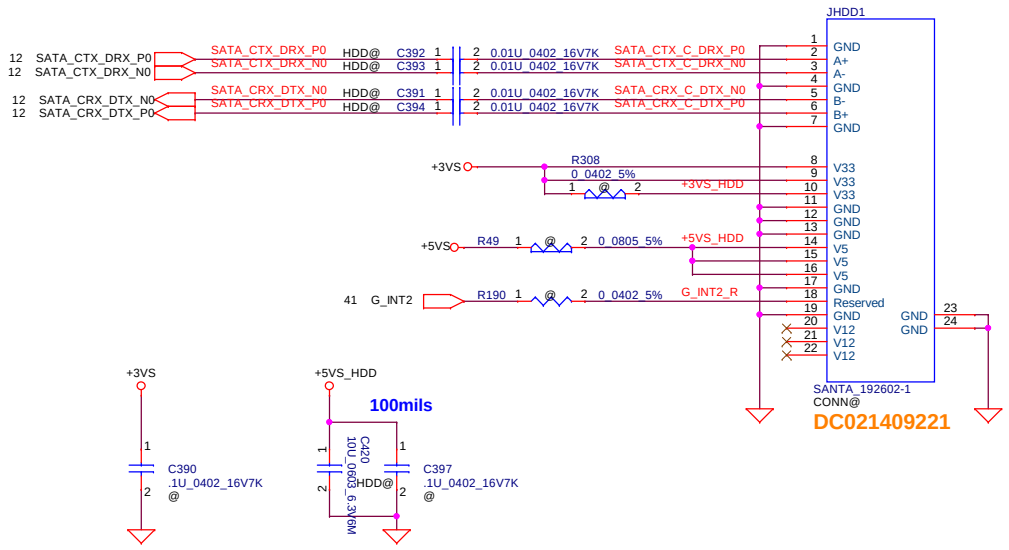
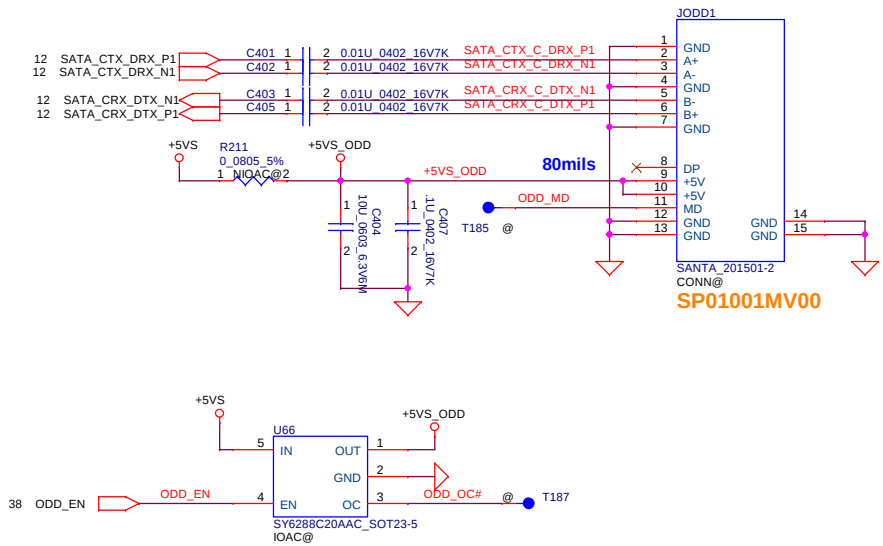
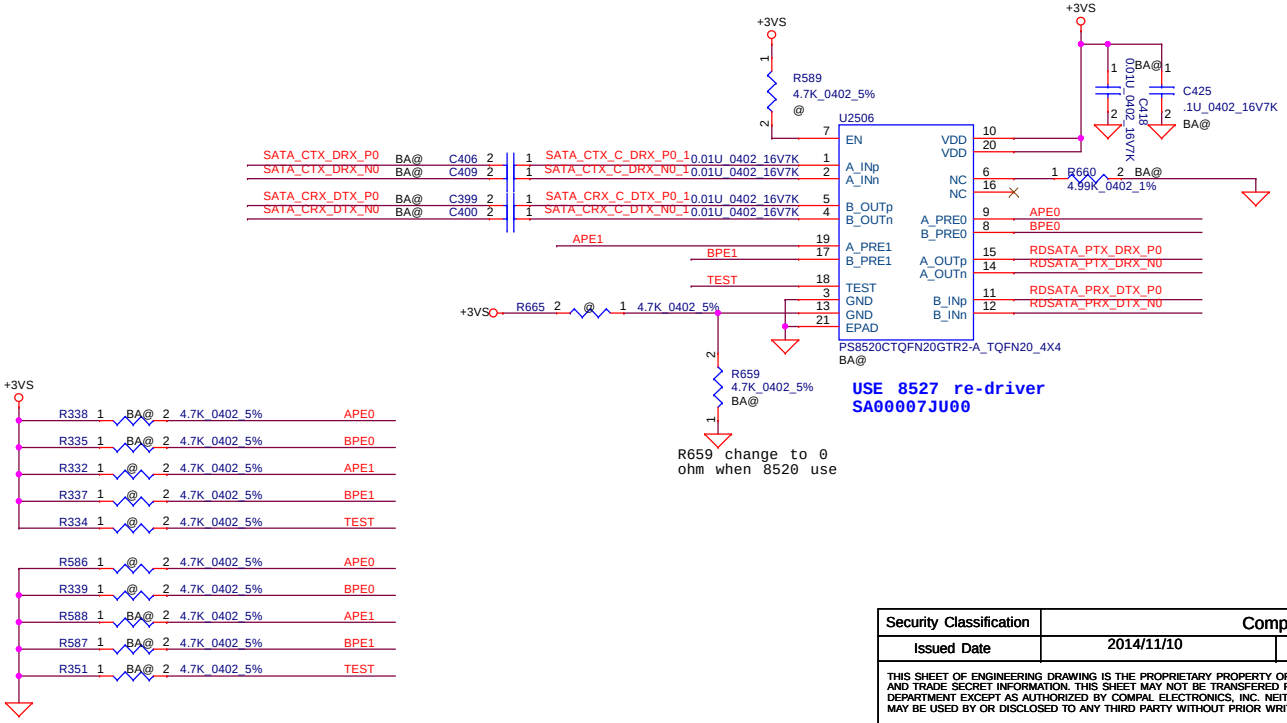
SATA HDD Conn.

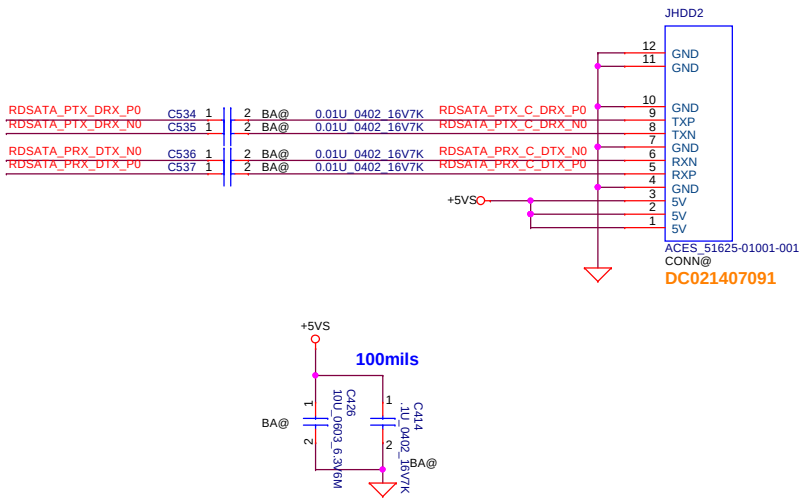


SATA ODD Conn.





SATA HDD Conn.



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Compal Electronics, Inc.

Title: HDD/ODD/ HDD Re-Driver

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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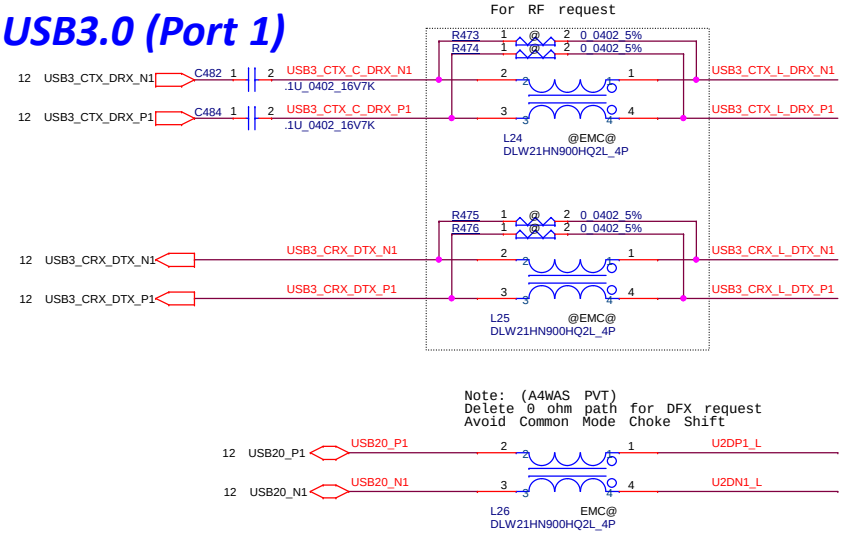
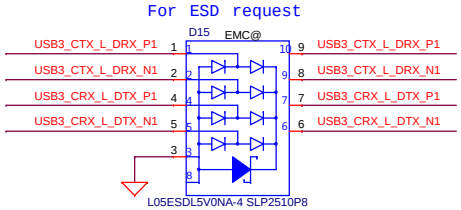
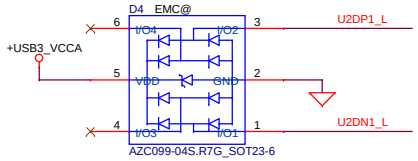
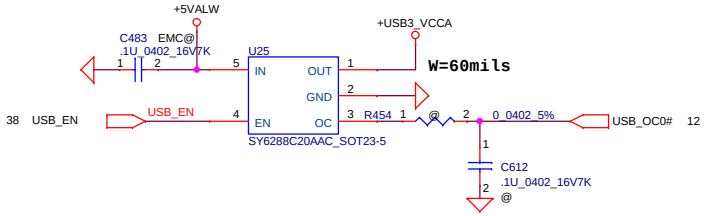
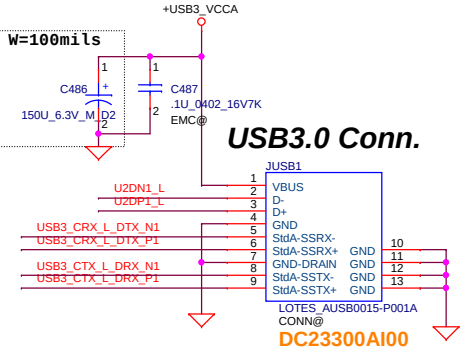
USB3.0 (Port 1)



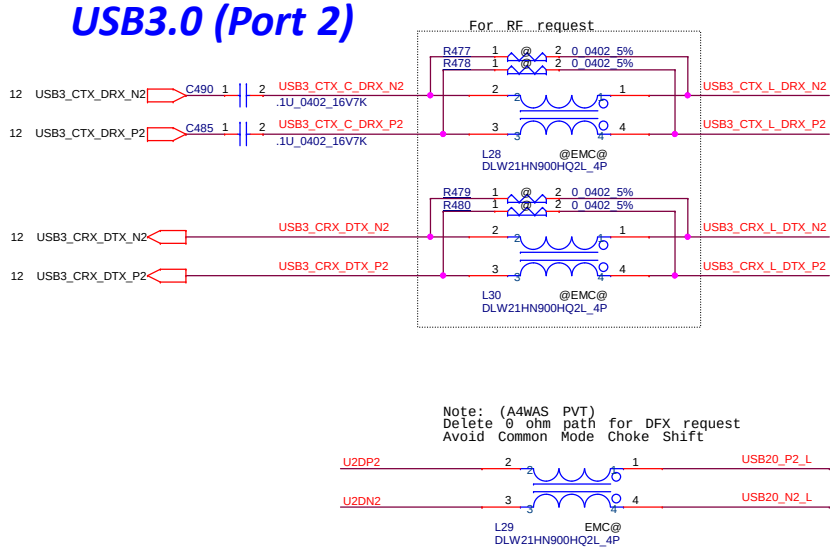


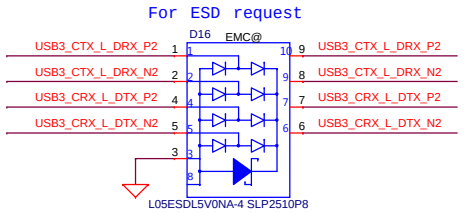


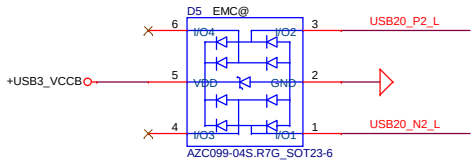


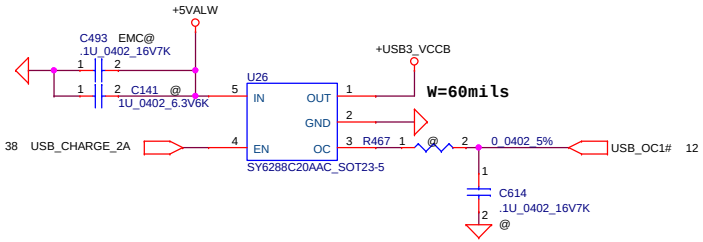


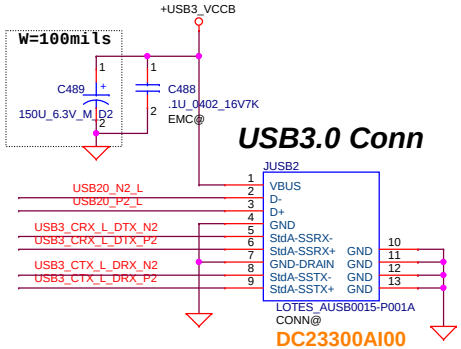
USB3.0 (Port 2)



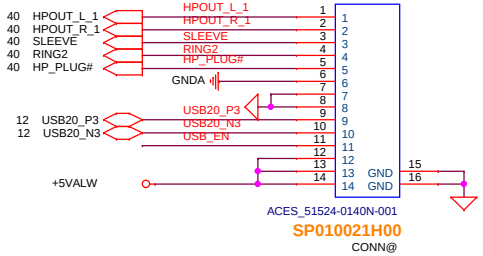






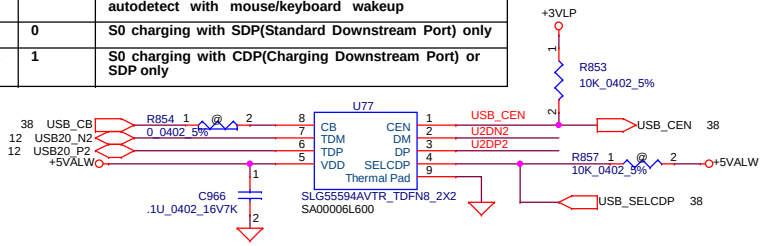


USB/B (USB Port 3, + AUDIO)



USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



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Title: USB3.0 Conn/USB_B

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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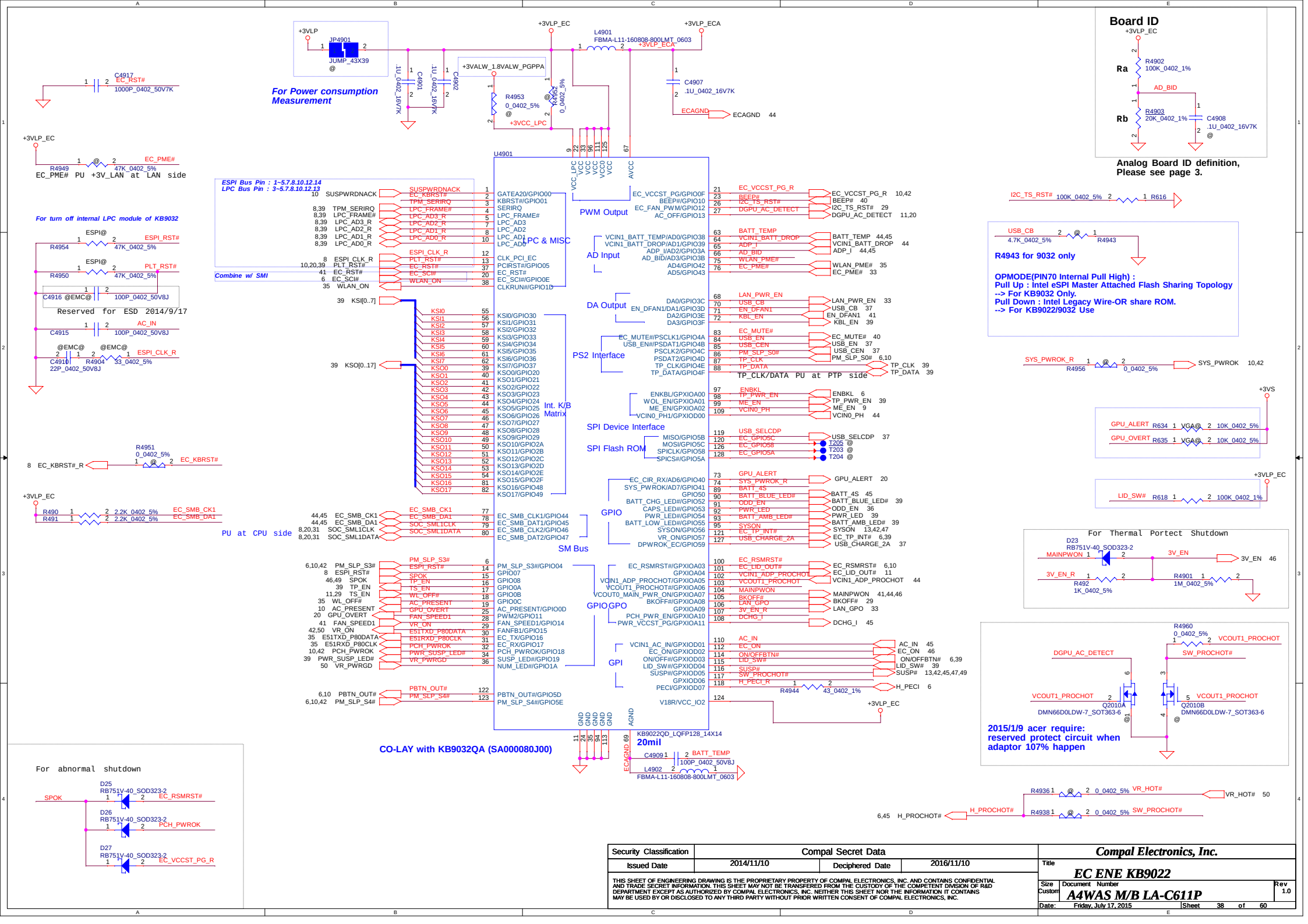

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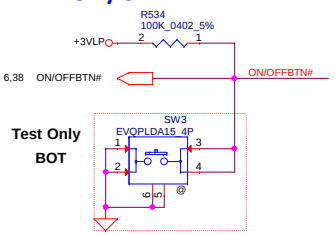
Title: EC ENE KB9022

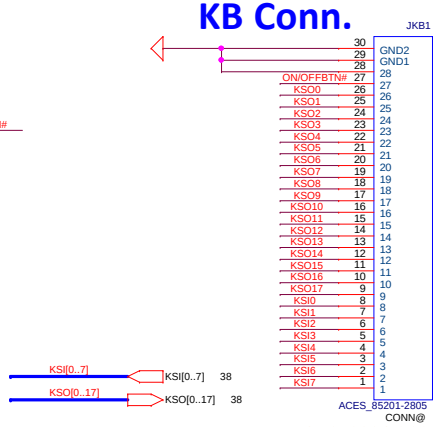
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Friday, July 17, 2015 | Sheet 38 of 60

ON/OFF BTN

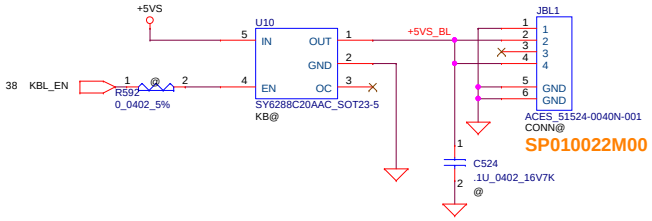


KB Conn.



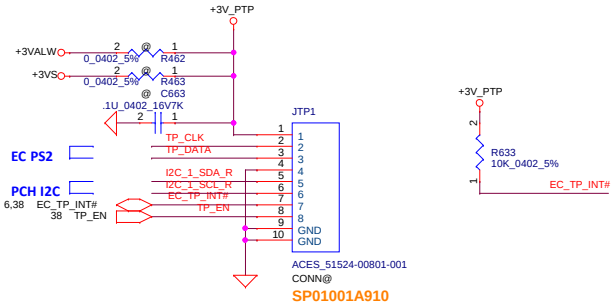
SP01000GO00

KB BackLight Conn. Reserve



SP010022M00

TP/B Conn.



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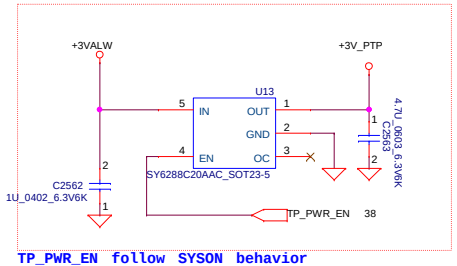
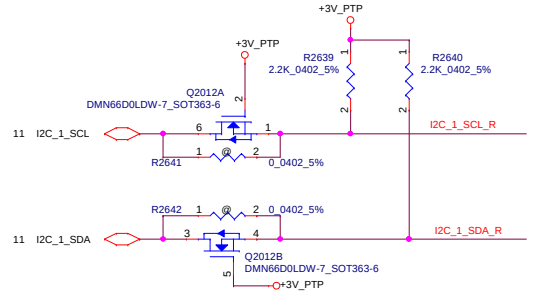
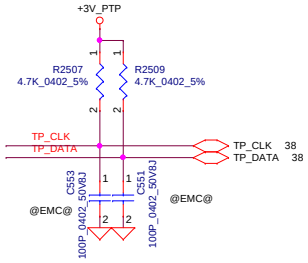
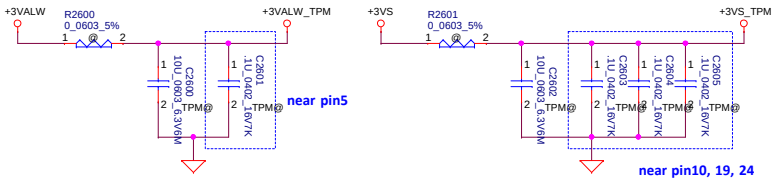


TP_PWR_EN follow SYSON behavior

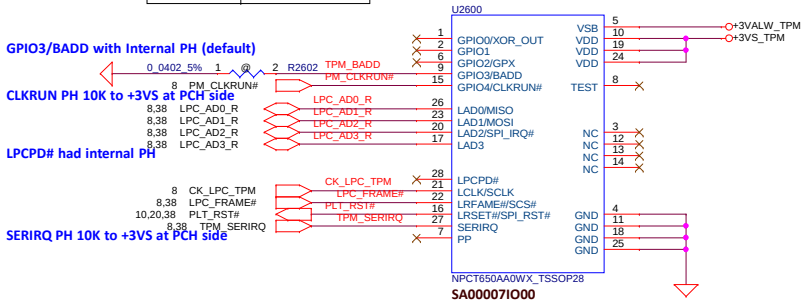


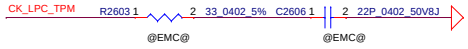


TPM Board for 2015

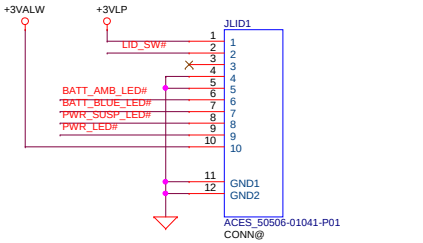


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh





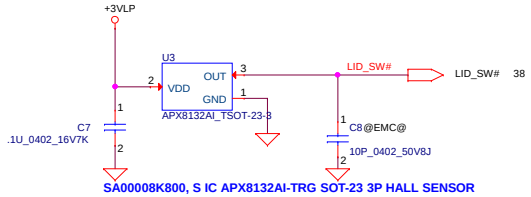
Lid Switch 2 (reserve for 15")



SP01001ER00
ACES_50506-01041-P01_10P-NPM

Lid Switch

(Hall Effect Switch)



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

LED

Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

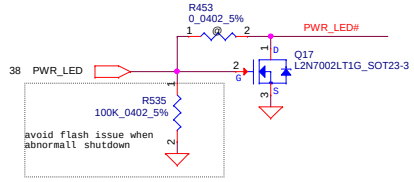
Vf @ 5 mA :

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

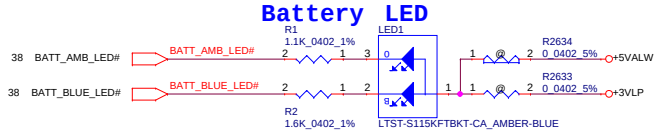
CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080

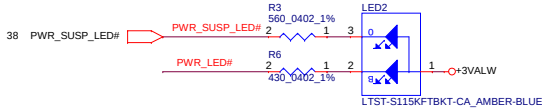
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080



Battery LED



Power LED



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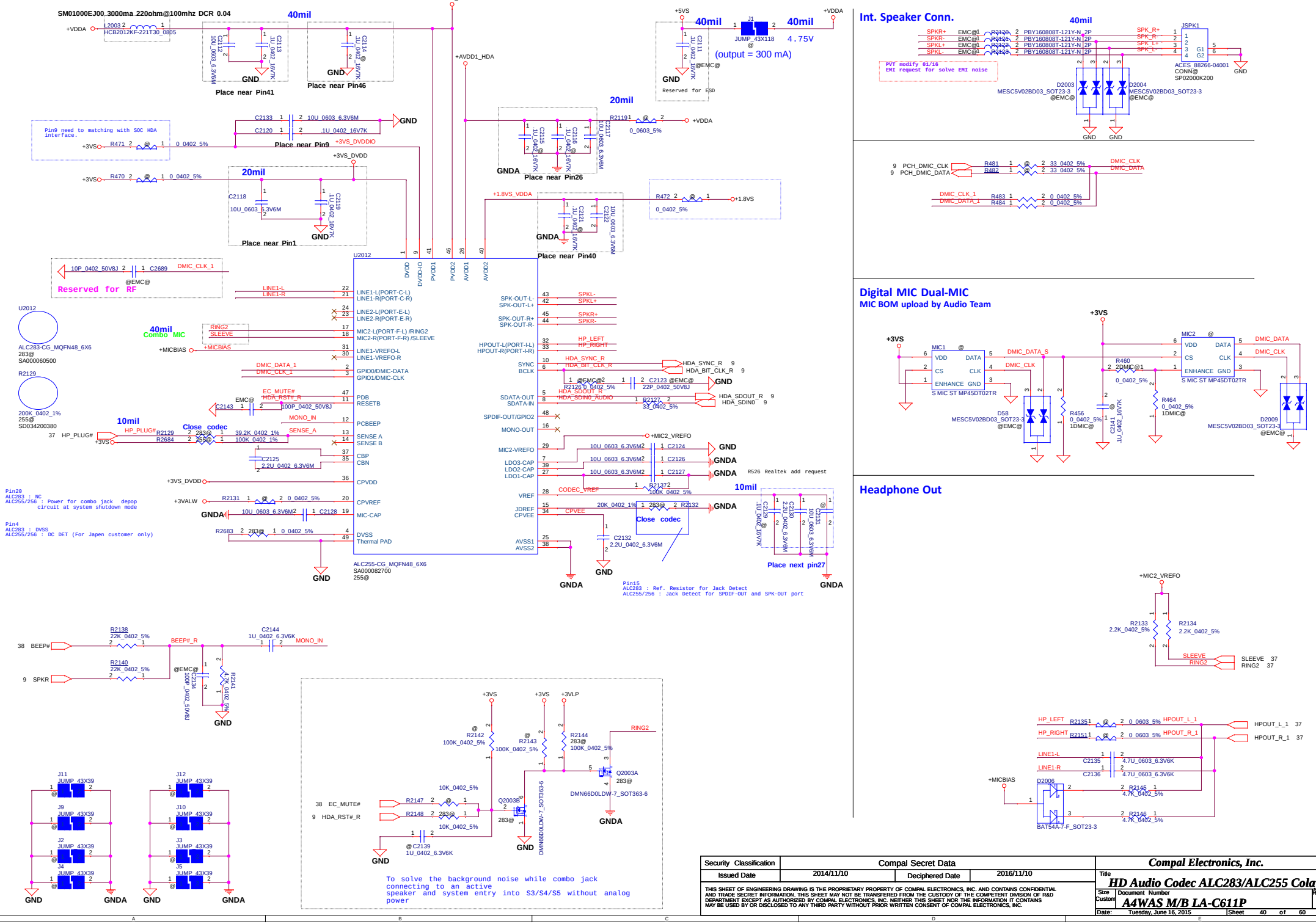
Compal Electronics, Inc.

Title: KB & TP & TPM Connector & LED

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Monday, June 22, 2015 | Sheet 39 of 60

HD Audio Codec



Int. Speaker Conn.

Digital MIC Dual-MIC

MIC BOM upload by Audio Team

Headphone Out

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: **HD Audio Codec ALC283/ALC255 Colay**

Size: Custom | Document Number: **A4WAS M/B LA-C611P** | Rev: 1.0

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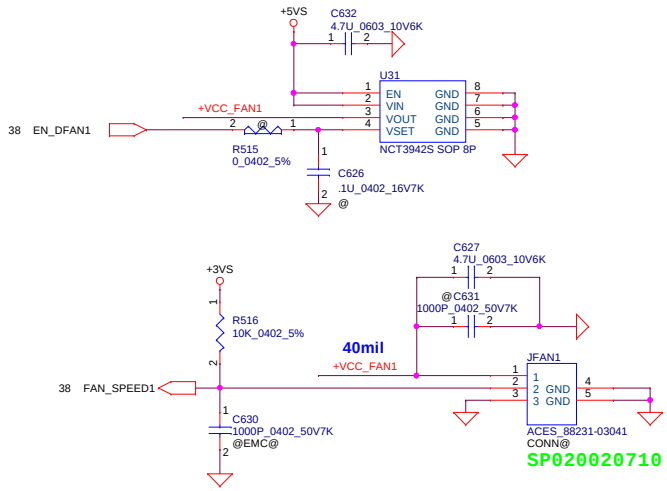
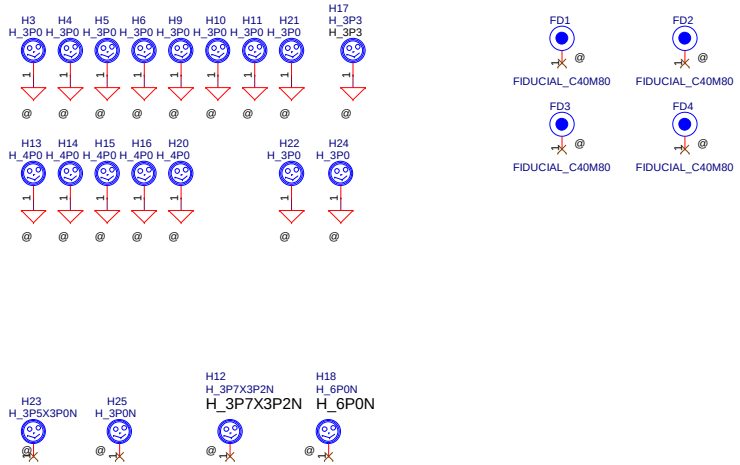
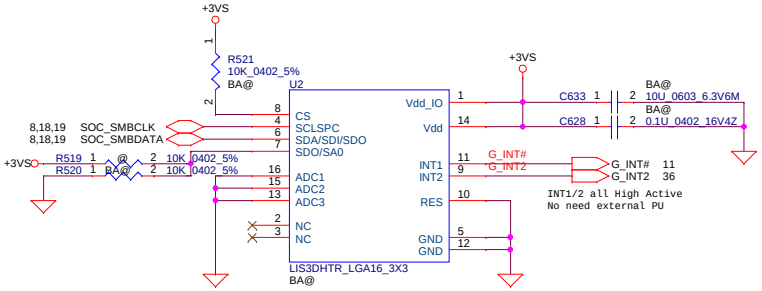
FAN1 Conn



Screw Hole

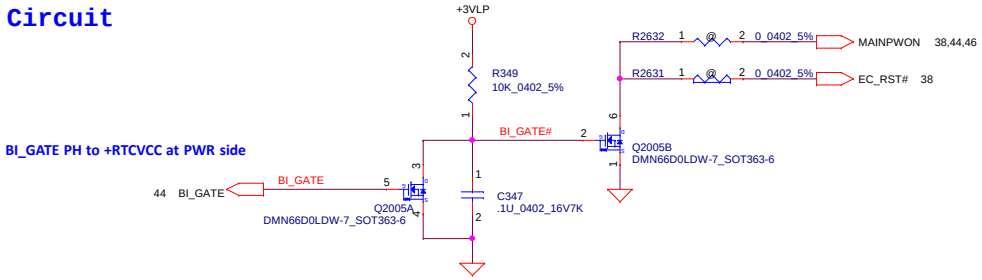


G-Sensor reserved for BA serial



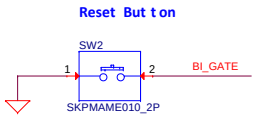
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

Reset Circuit

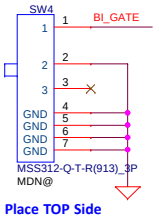


Debug SW

Reset Button

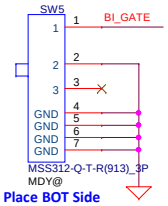


BI SW



1-2 : Battery Off
2-3 : Battery ON

BI SW



Reserved for memory door only

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: FAN & Screw Hole & G-Sensor

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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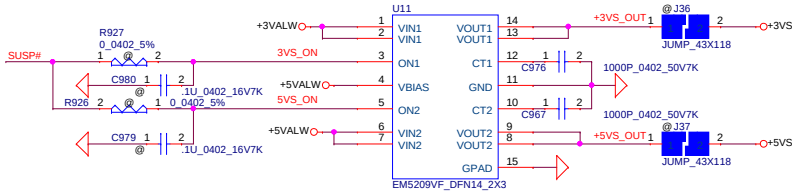
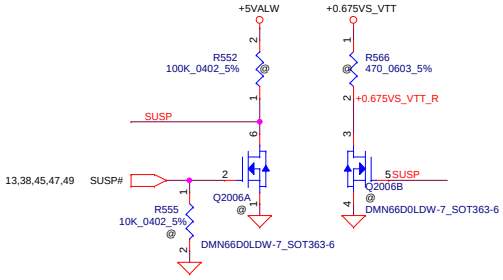
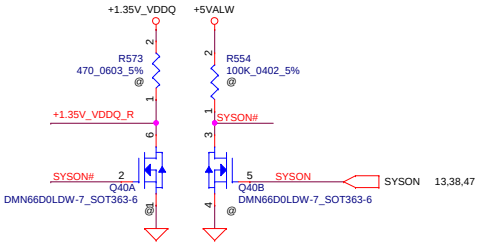
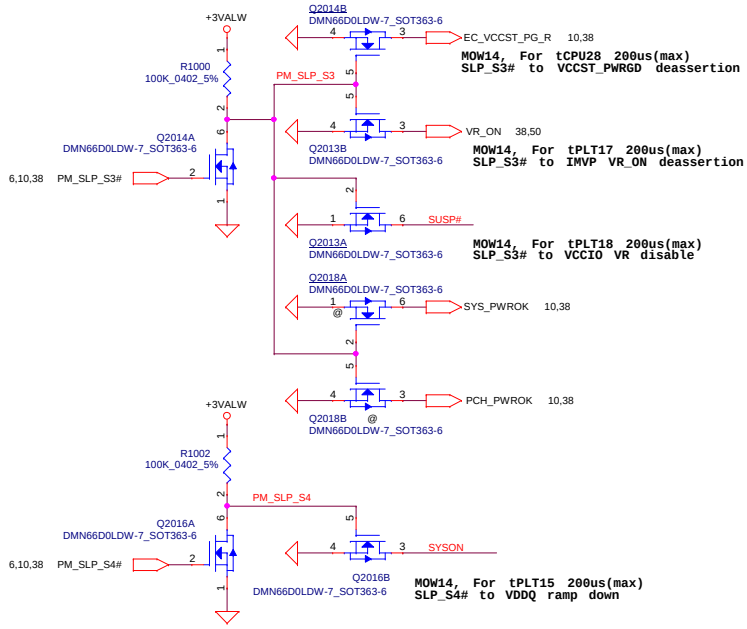
DC & VGA Interface



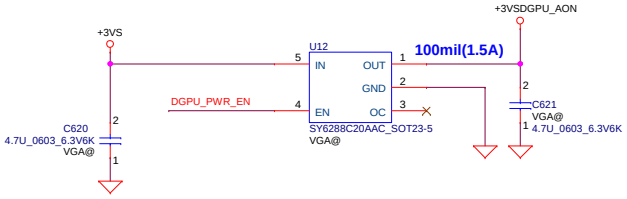


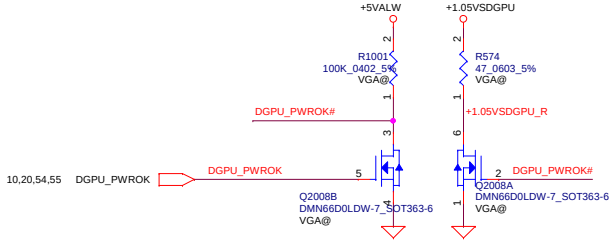


For Power ON/Off Sequence

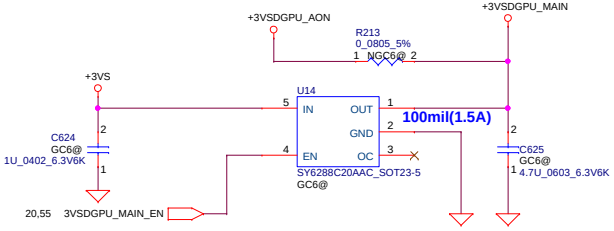


+3VS to +3VSDGPU_AON for GPU

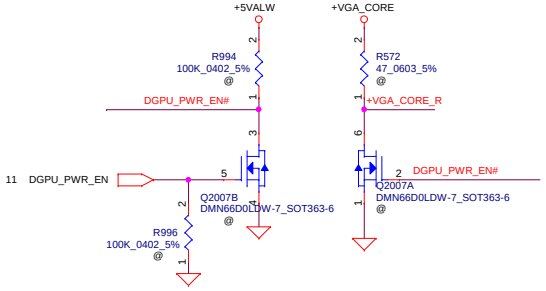


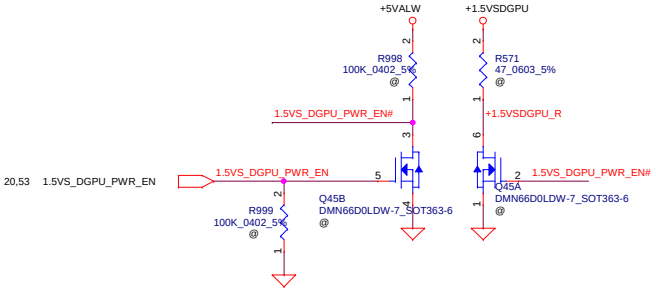


+3VS to +3VSDGPU_MAIN for GC6-2.0



3VSDGPU_MAIN_EN From GPU





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Compal Electronics, Inc.

Title: **DC Interface**

Size: Custom | Document Number: **A4WAS M/B LA-C611P** | Rev: 1.0

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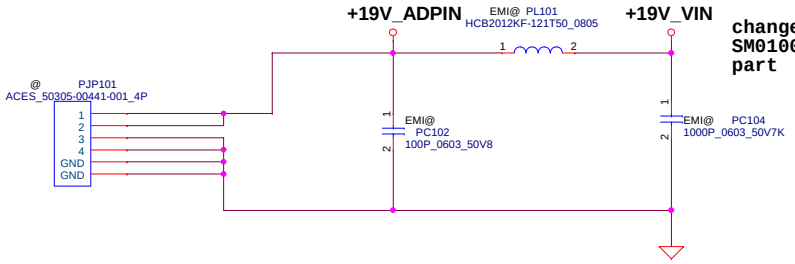
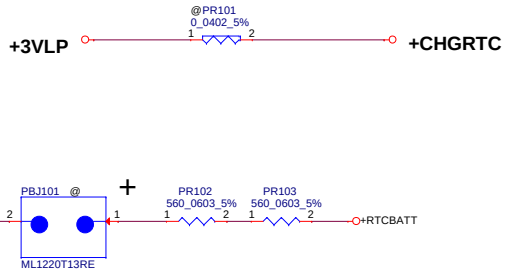


change PL101 SM01000C000 to comm part SM01000P200

2011/10/13
for EN9012 application, delete the 51_ON# circuit

2011/10/12
delete the pre-CHG circuit



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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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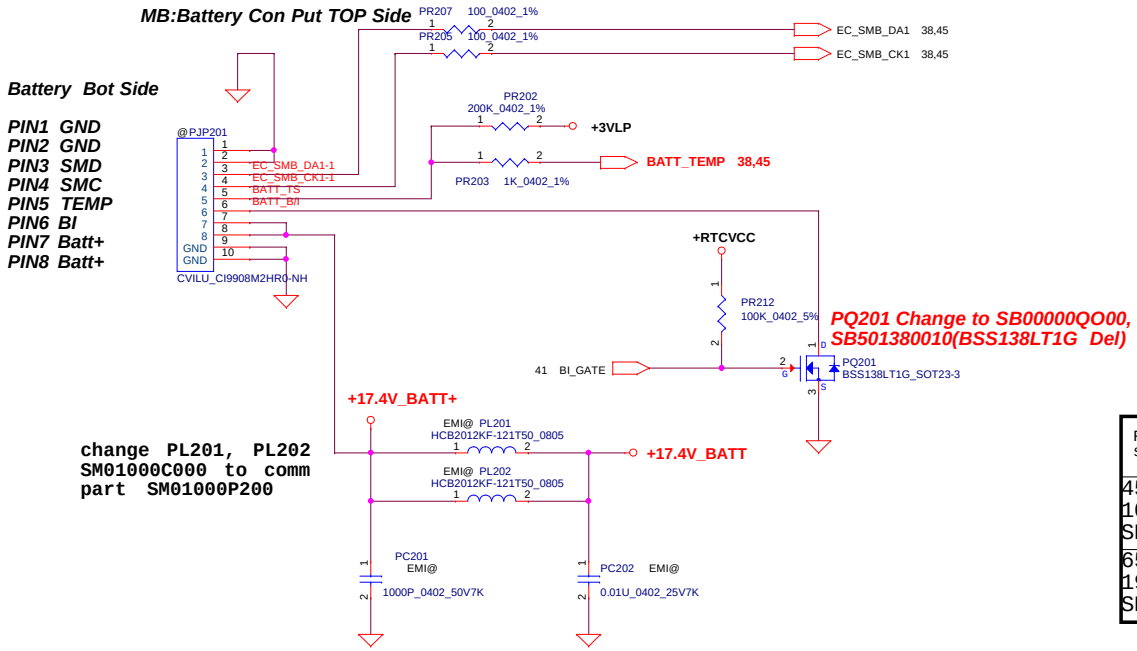
Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

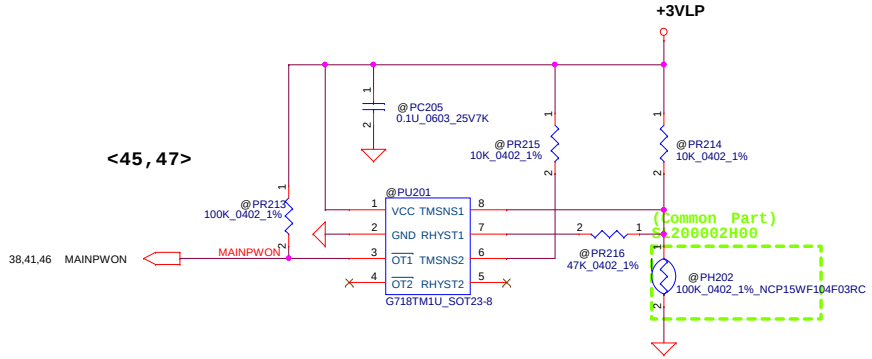
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 43 of 60

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



change PL201, PL202 SM01000C000 to comm part SM01000P200



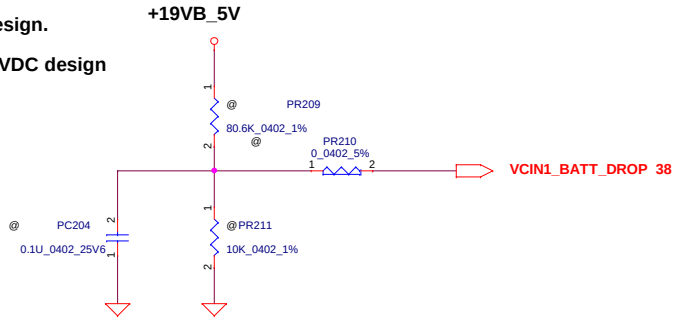
2014/09/25 update

For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm SD034100280	58.5W,0.61V	45W,0.47V
65W PR206 19.1K ohm SD034191280	84.5W,0.61V	65W,0.47V

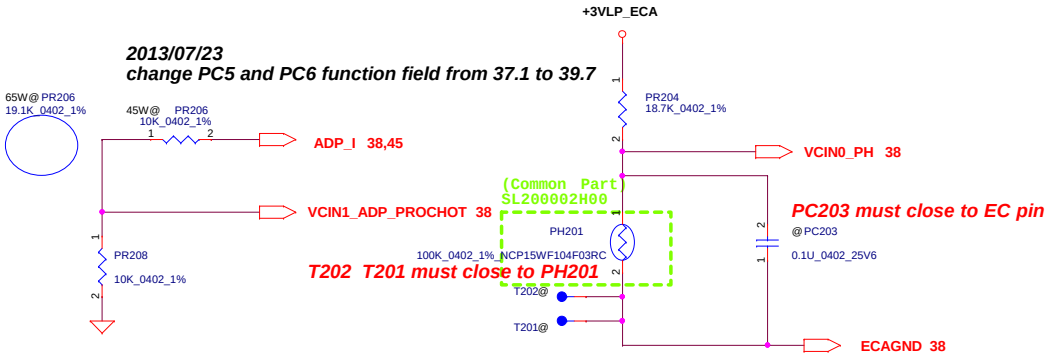
PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V



2013/07/23
change PC5 and PC6 function field from 37.1 to 39.7



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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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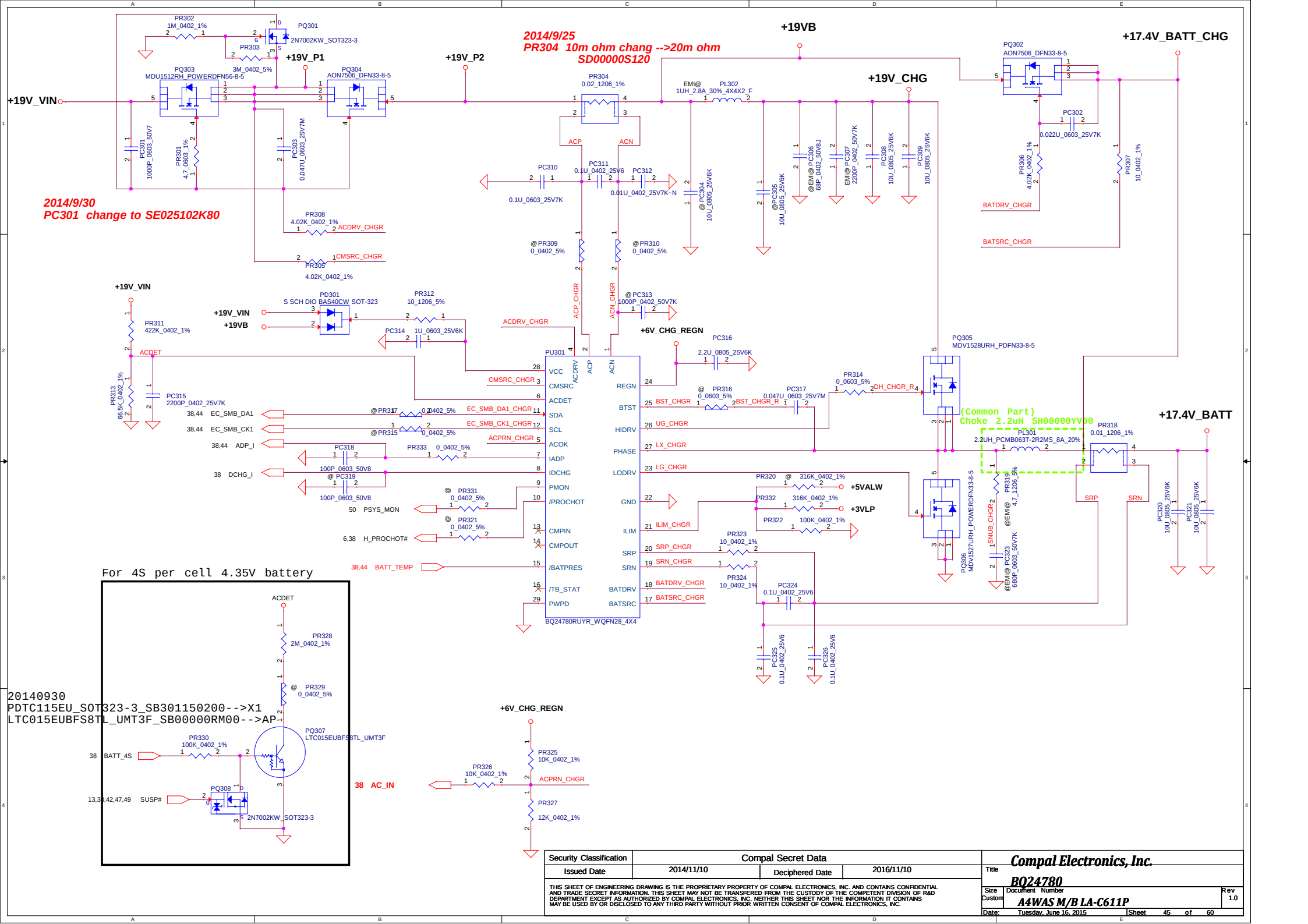
Compal Electronics, Inc.
Title: PWR-BATTERY CONN/OTP
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0
Date: Monday, June 22, 2015 | Sheet 44 of 60


2014/9/25
PR304 10m ohm chang -->20m ohm
SD00000S120
2014/9/30
PC301 change to SE025102K80
+19V_VIN
+19V_P1
+19V_P2
+19VB
+19V_CHG
+17.4V_BATT_CHG
+17.4V_BATT
+6V_CHG_REGN
PQ301 2N7002KW_SOT323-3
PQ303 MDU1512RH_POWERDFN56-8-5
PQ304 AON7506_DFN33-8-5
PQ302 AON7506_DFN33-8-5
PR304 0.02_1206_1%
PL302 1UH_2.8A_30%_4X4X2_F
PU301
BQ24780RUYR_WQFN28_4X4
PQ305 MDV1528URH_PDFN33-8-5
PQ306 MDV1527URH_POWERDFN33-8-5
PL301 2.2UH_PCMB063T-2R2MS_8A_20%
(Common Part)
Choke 2.2uH SH00000YV00
PR318 0.01_1206_1%
PD301 S SCH DIO BAS40CW SOT-323
For 4S per cell 4.35V battery
PQ307 LTC015EUBFS8TL_UMT3F
PQ308 2N7002KW_SOT323-3
38 BATT_4S
13,30,42,47,49 SUSP#
38 AC_IN
20140930
PDTC115EU_SOT323-3_SB301150200-->X1
LTC015EUBFS8TL_UMT3F_SB00000RM00-->AP
Security Classification
Compal Secret Data
Issued Date
2014/11/10
Deciphered Date
2016/11/10
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Compal Electronics, Inc.
Title
BQ24780
Size Custom
Document Number
A4WAS M/B LA-C611P
Rev 1.0
Date: Tuesday, June 16, 2015
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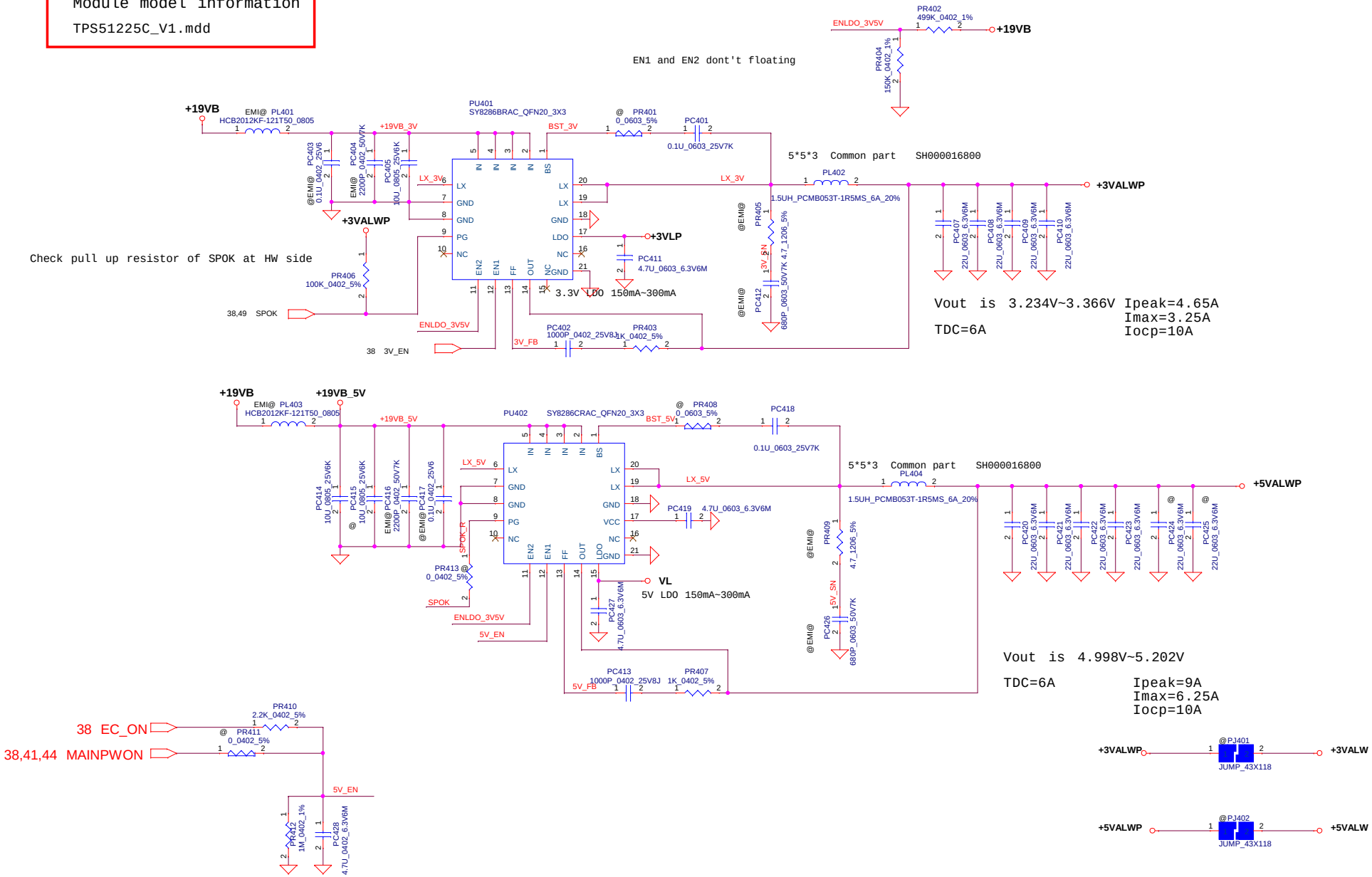
Module model information

TPS51225C_V1.mdd



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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

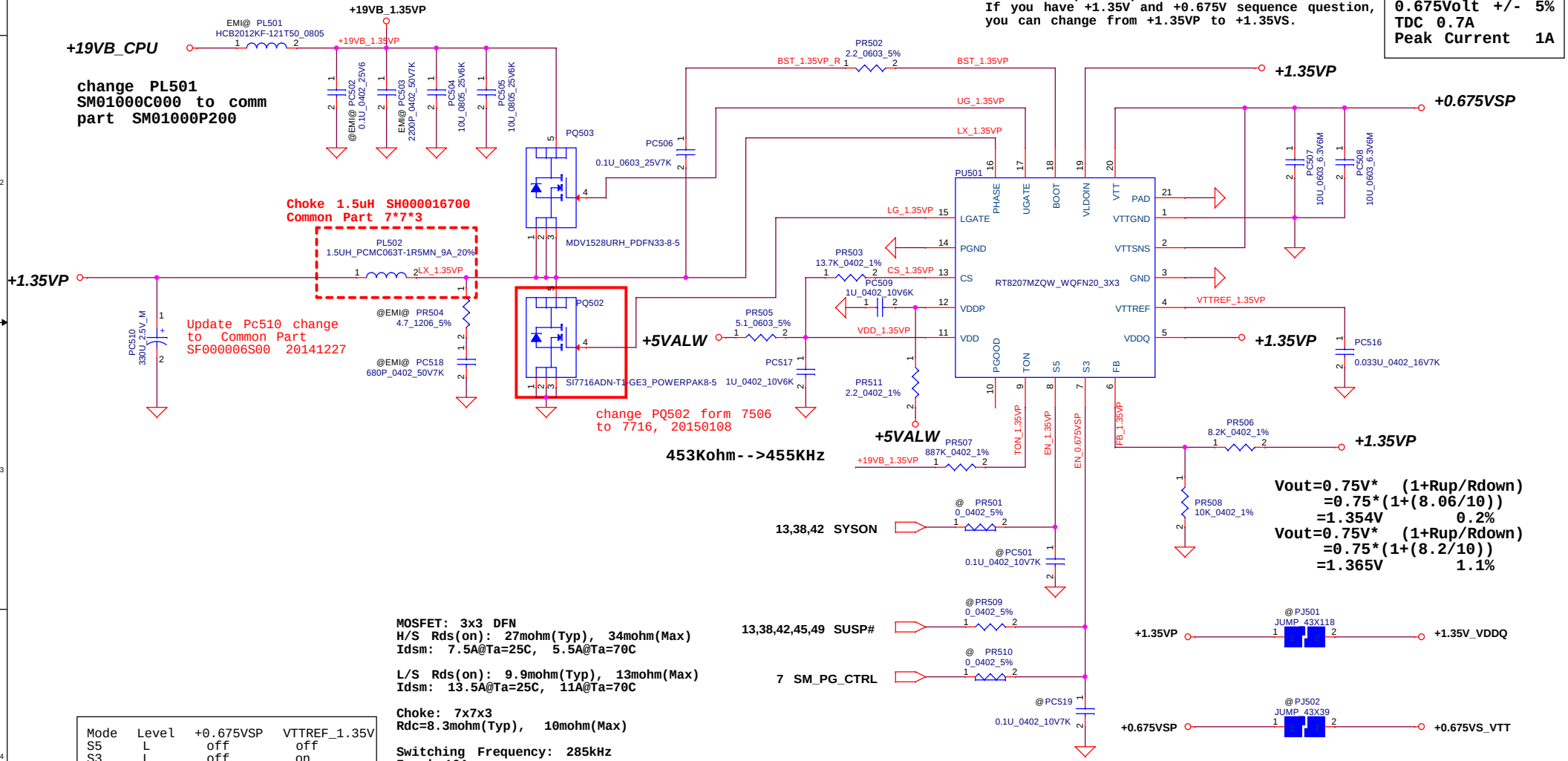
Date: Tuesday, June 16, 2015 | Sheet 46 of 60

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V
MOSFET footprint: SIS412DN

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: RT8207P

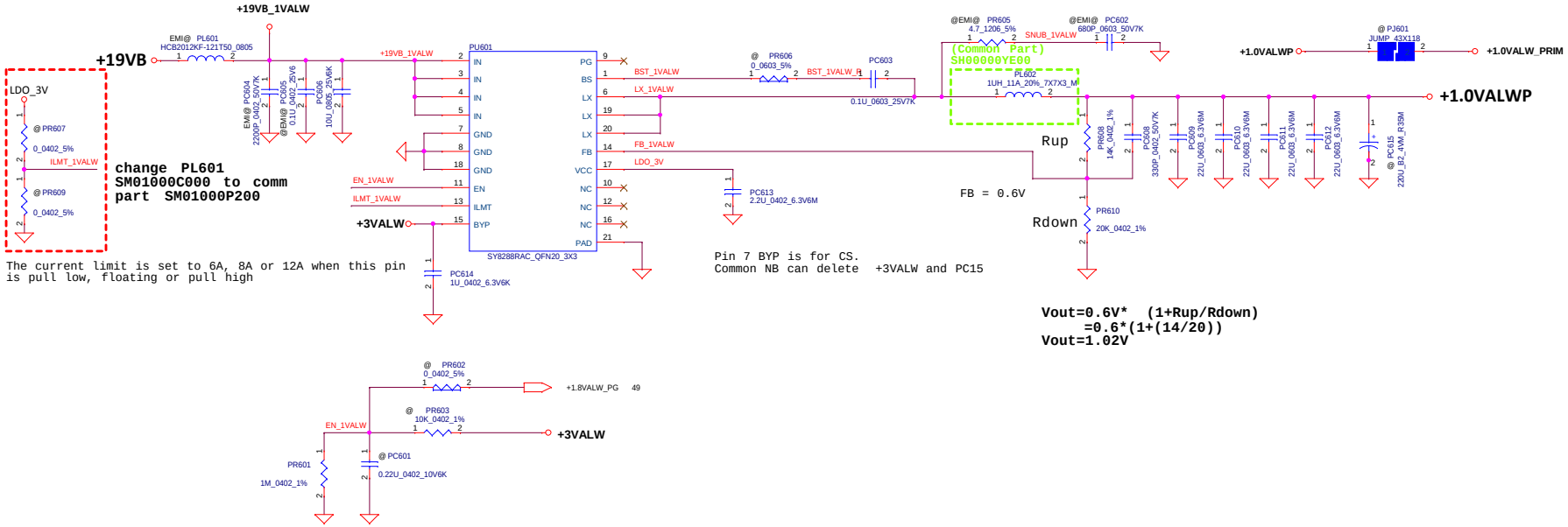
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 47 of 60

Module model information

SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



change PL601 SM01000C000 to comm part SM01000P200

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

FB = 0.6V

Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(14/20))
Vout=1.02V

Function Field :
VCCEDPIO : IC-35.21 , others - 35.22
VCCEDRAM : IC-35.25 , others - 35.26

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

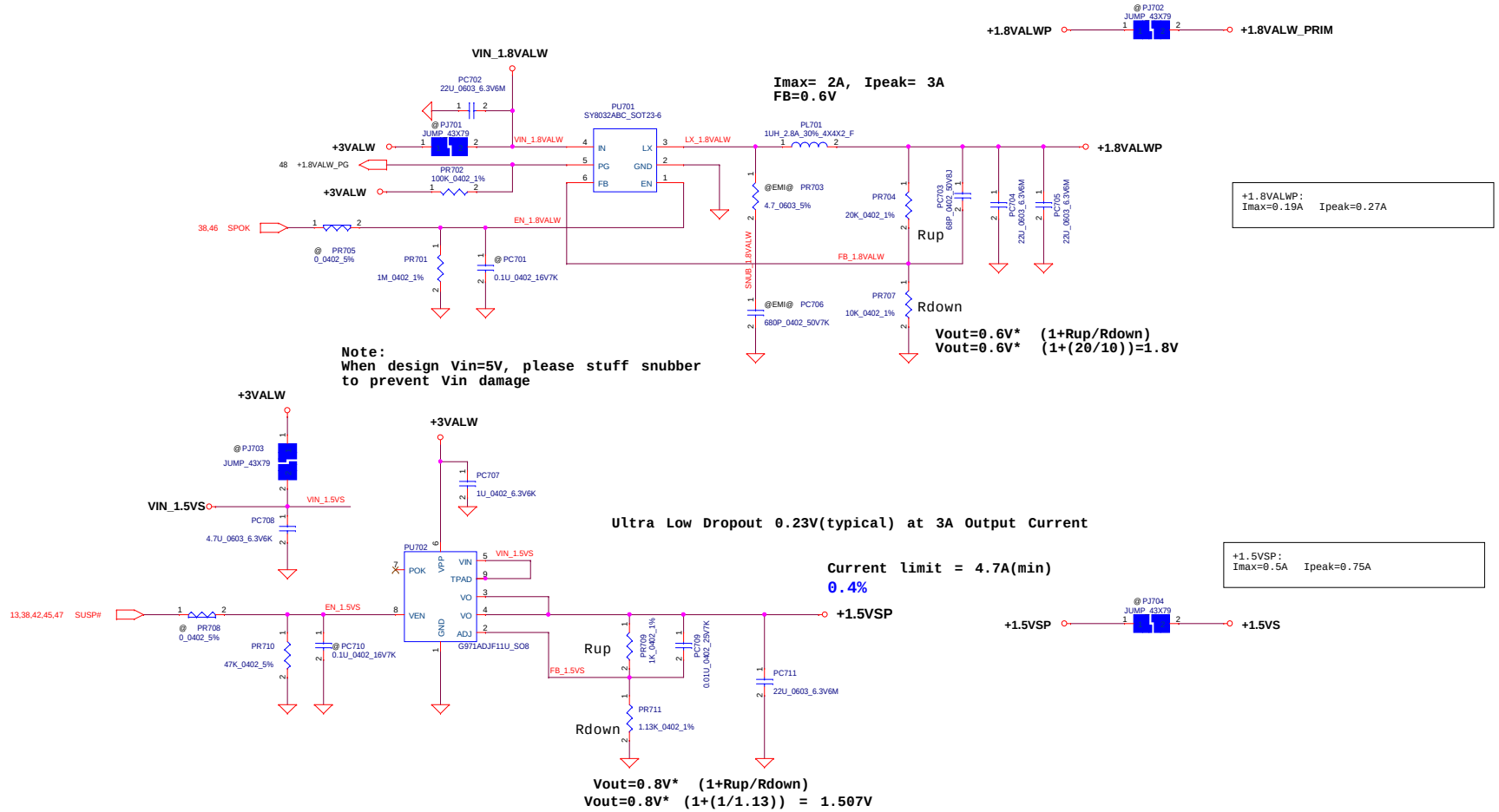
Title: VCCP

Size: C | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, July 14, 2015 | Sheet 48 of 60

Module model information

SY8032_V2.mdd



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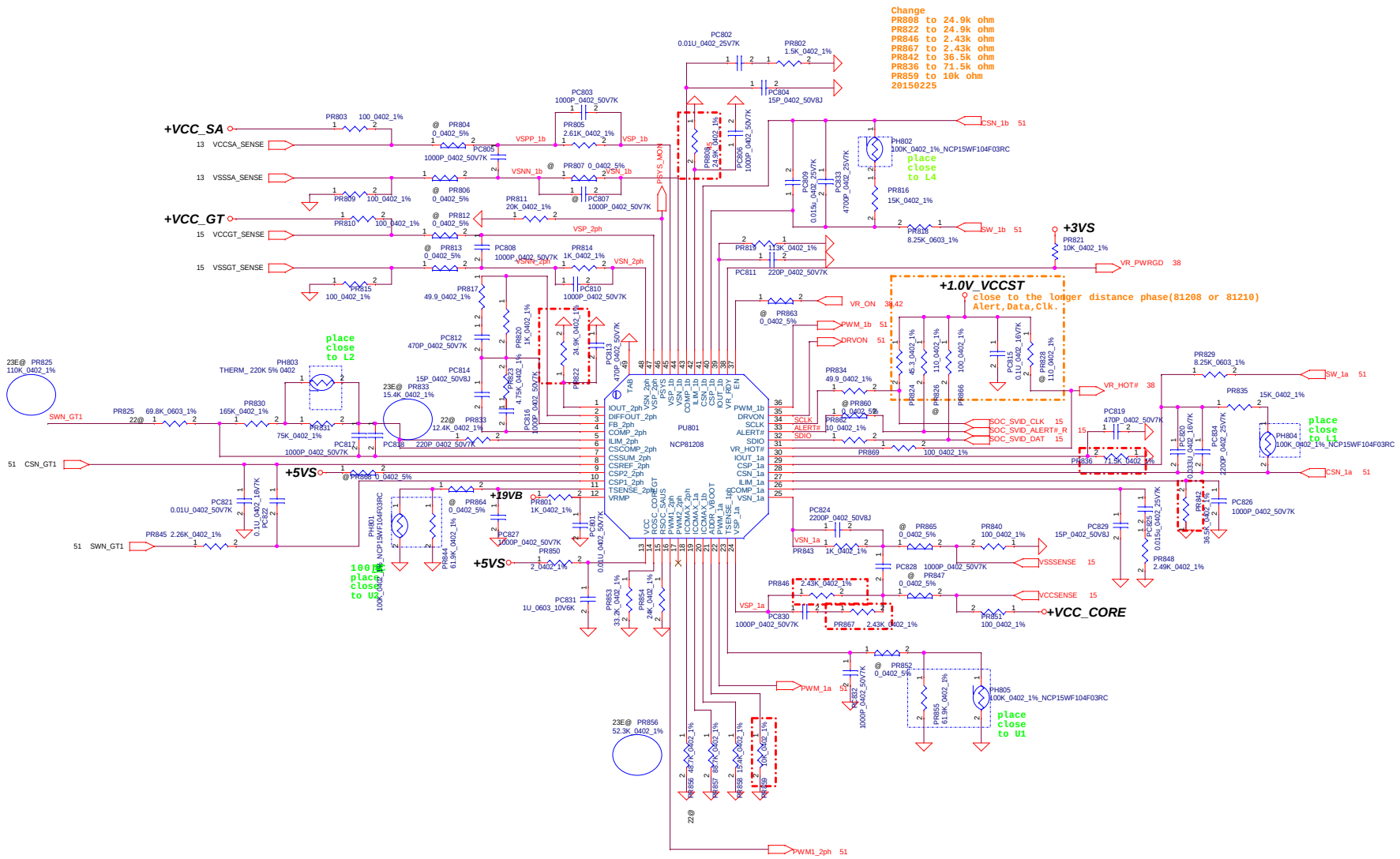
Compal Electronics, Inc.

Title: SY8032

Size: C | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, July 14, 2015 | Sheet 49 of 60



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: IMVP8, NCP81206

Size: C | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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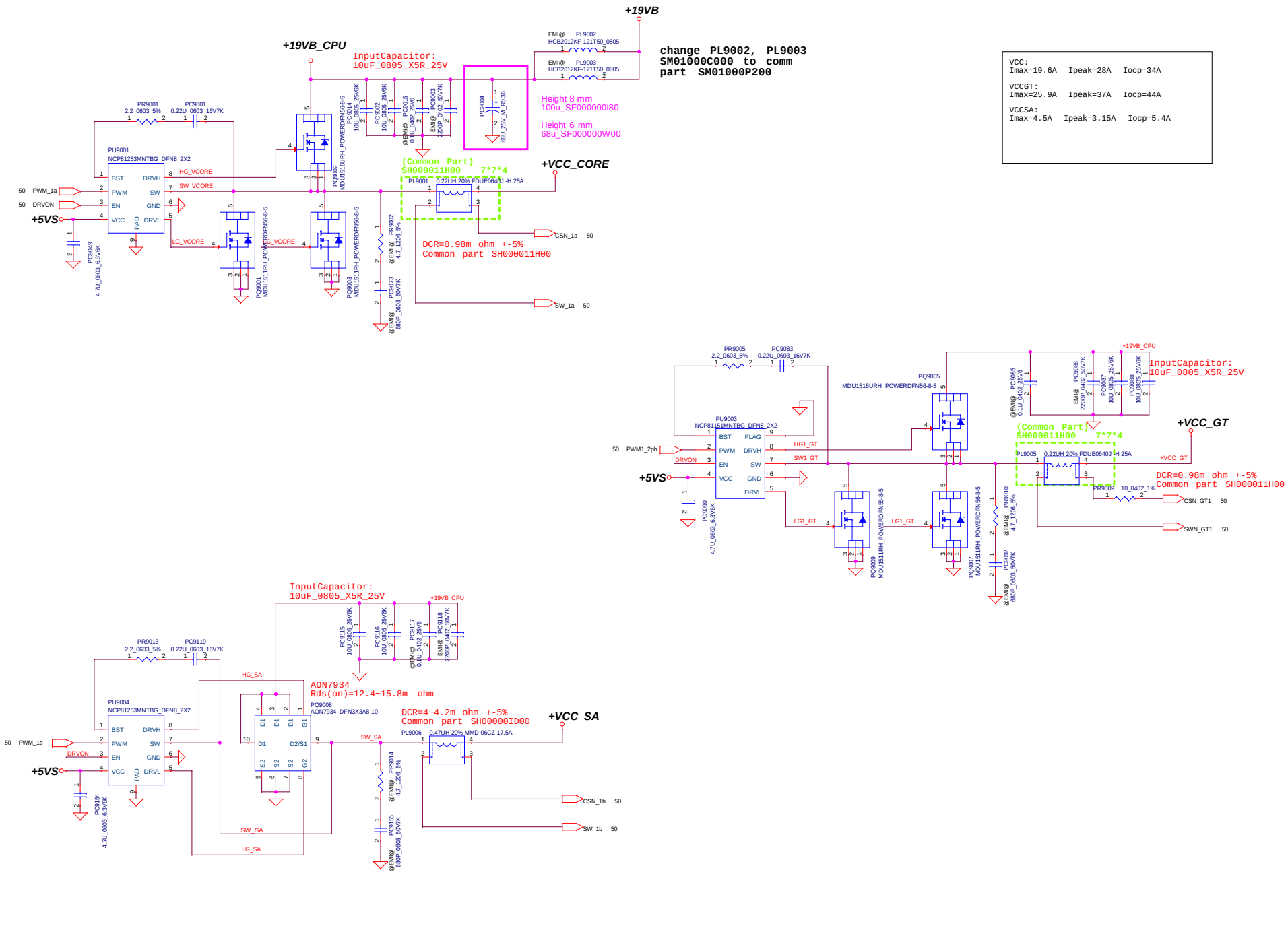

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Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
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Date: Tuesday, June 16, 2015 Sheet 51 of 60

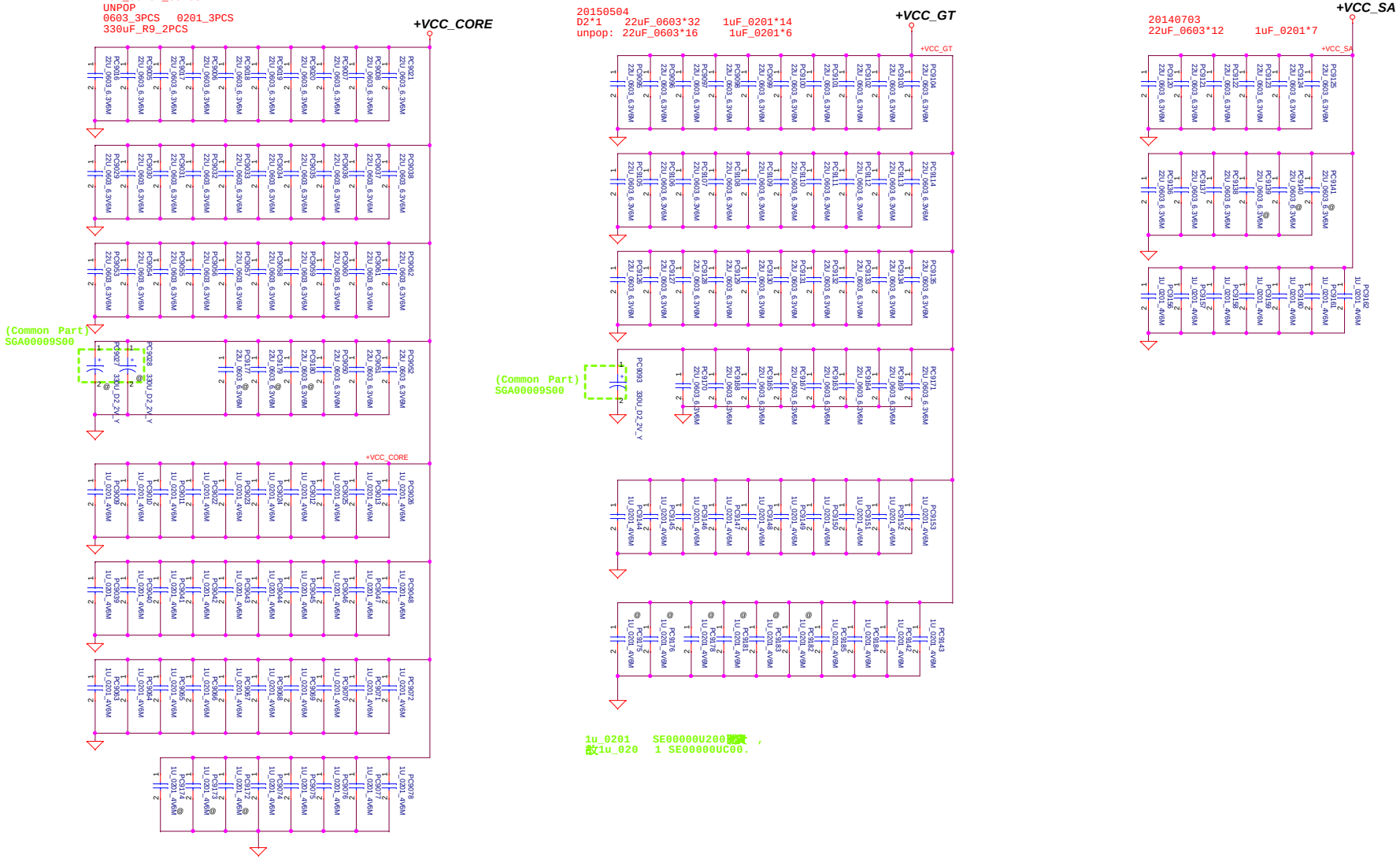
543016_543016_SKL_PDG_UY_1_0_pub
Total VCORE Output Capacitor:
2014/09/23
22uF_0603_33PCS
1uF_30201_35PCS
UNPOP
0603_3PCS 0201_3PCS
330uF_R9_2PCS

20140703
23E: D2*2 22uF_0603*29 1uF_0201*12
22: D2*1 22uF_0603*26 1uF_0201*12

20140923
D2*1 22uF_0603*38 1uF_0201*14
unpop: 22uF_0603*10 1uF_0201*6

20150504
D2*1 22uF_0603*32 1uF_0201*14
unpop: 22uF_0603*16 1uF_0201*6

20140703
22uF_0603*12 1uF_0201*7



1u_0201 SE00000U200 , 敷1u_020 1 SE00000UC00.

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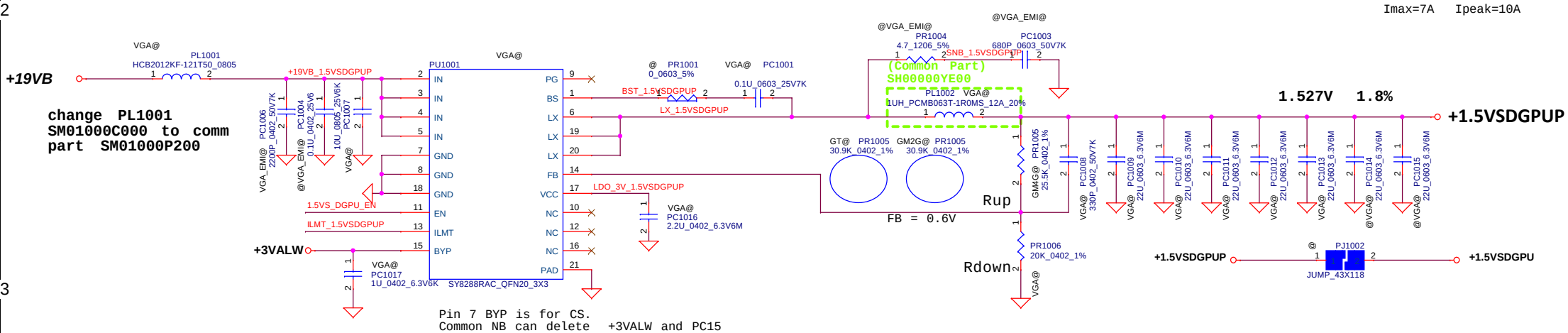
Compal Electronics, Inc.

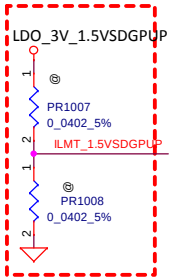
Title: Power Train

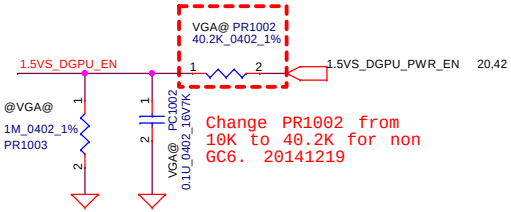
Size: C | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 52 of 60



Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15





VGA	Brand Name	VRAM Size	Voltage
N16S-GT	NV940	2GB	1.5V(or 1.35V)
		4GB	1.5V(or 1.35V)
N16V-GM	NV920	2GB	1.5V(or 1.35V)
		4GB	Only 1.35V

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.365V

Vout=0.6V* (1+(25.5/20))=1.356

Vout=0.6V* (1+(30.9/20))=1.527

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

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Compal Electronics, Inc.

Title: 1.5VSDGPUP

Size: A3 | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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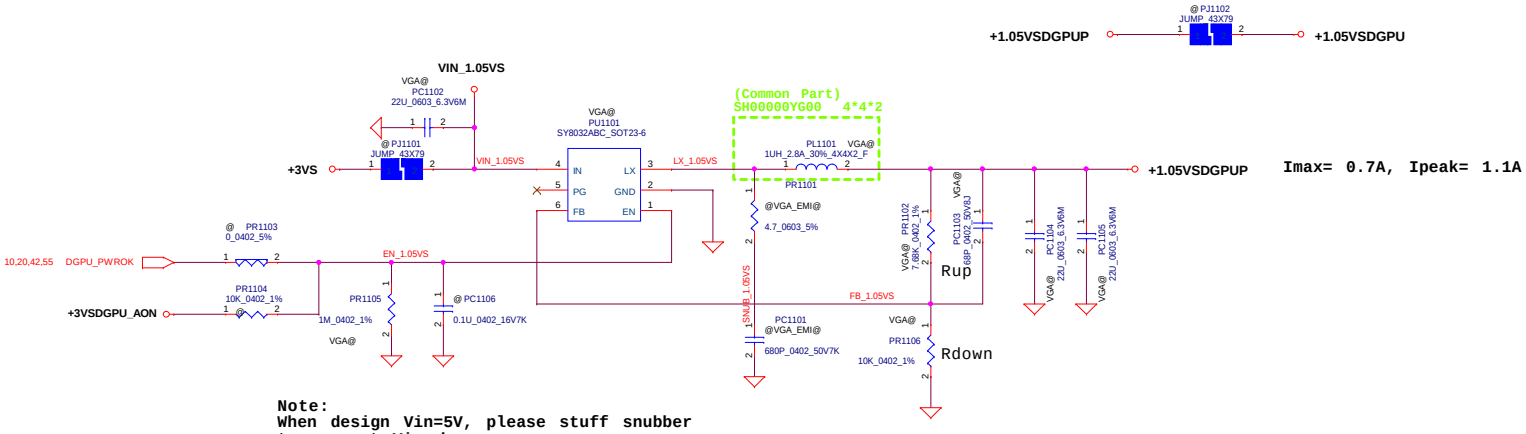
Module model information

SY8032_V2.mdd



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.87/10)=1.072 (2.1%)

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Compal Electronics, Inc.

Title: SY8032

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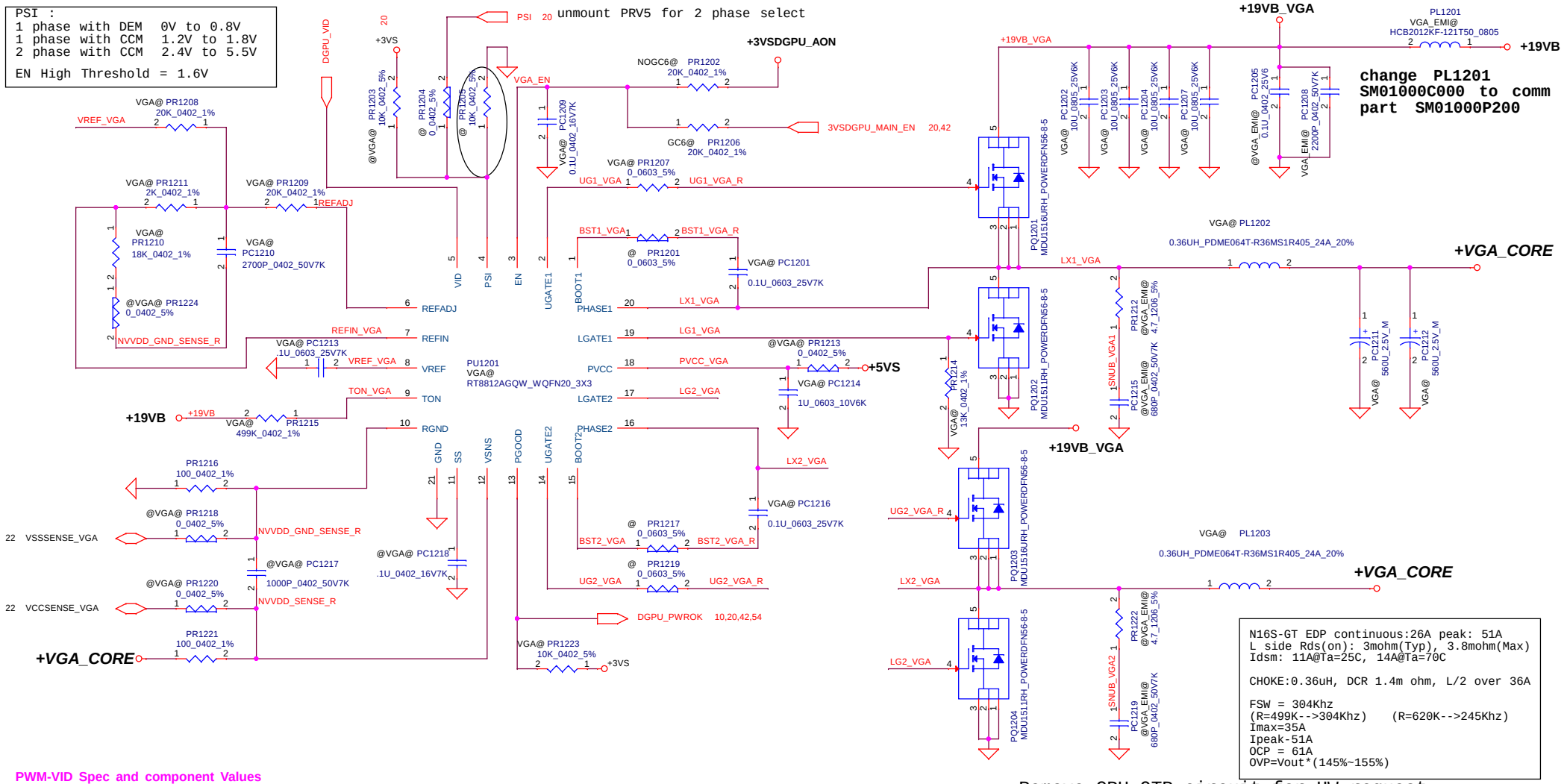
PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

unmount PRV5 for 2 phase select

change PL1201 SM01000C000 to comm part SM01000P200



N16S-GT EDP continuous:26A peak: 51A
L side Rds(on): 3mohm(Typ), 3.8mohm(Max)
Idsm: 11A@Ta=25C, 14A@Ta=70C

CHOKE:0.36uH, DCR 1.4m ohm, L/2 over 36A

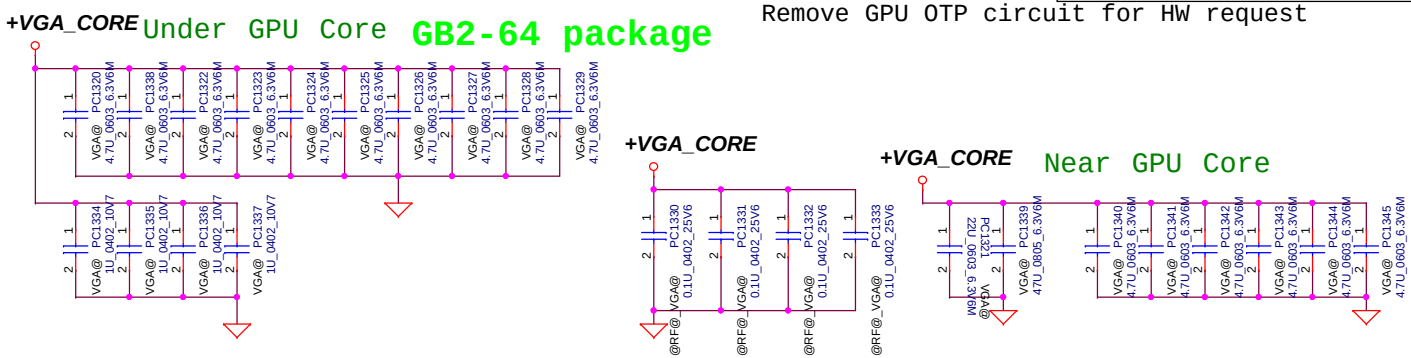
FSW = 304Khz
(R=499K-->304Khz) (R=620K-->245Khz)
Imax=35A
Ipeak-51A
OCP = 61A
OVP=Vout*(145%~155%)

Remove GPU OTP circuit for HW request

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR	20K	39K	27K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2=PR1209 +PR1212	PR	18K	24K	6.2K
	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

N16S-GT
N16V-GM



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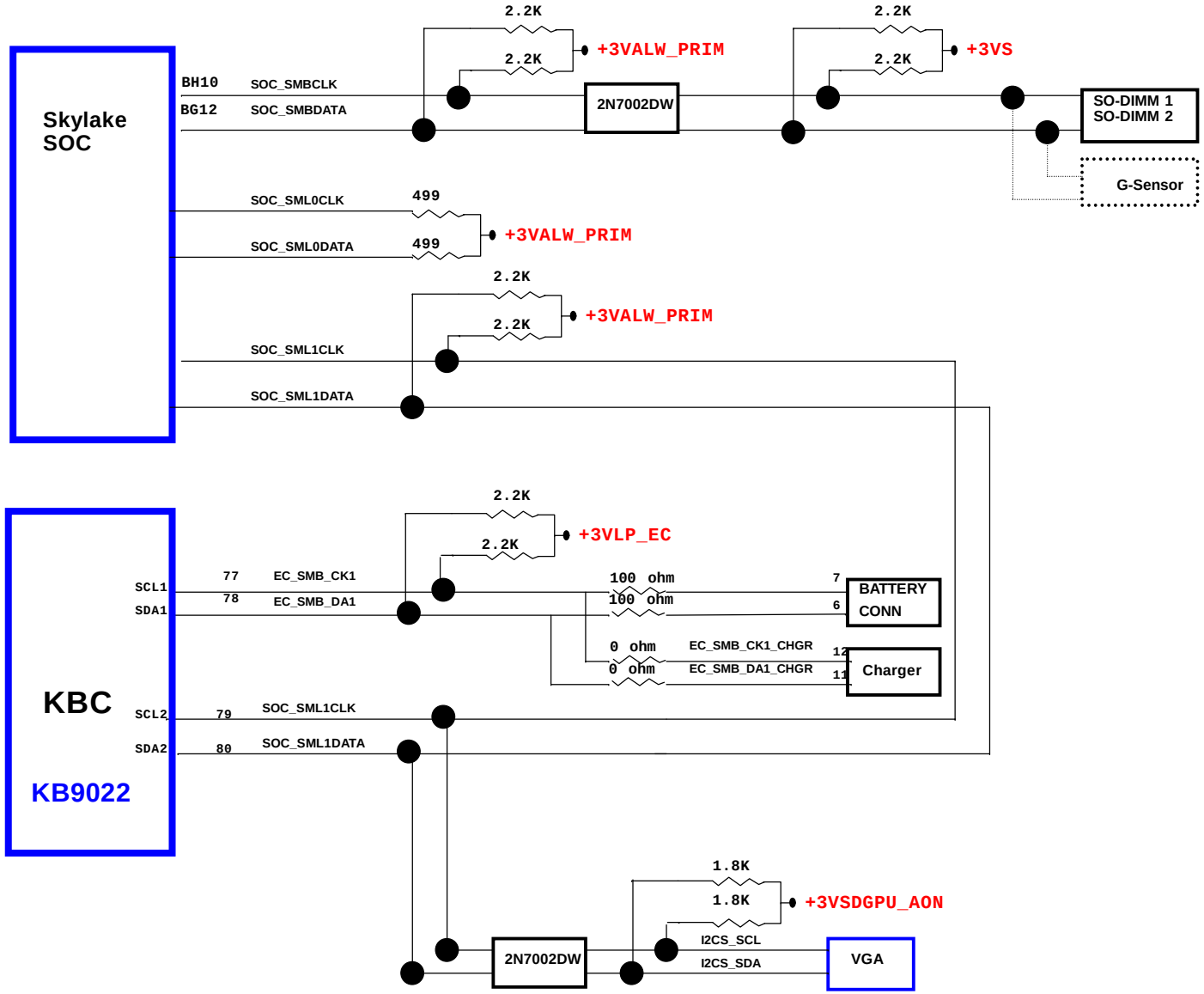
Compal Electronics, Inc.

Title: NVIDIA VGA CORE

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Monday, June 22, 2015 | Sheet 55 of 60



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Compal Electronics, Inc.

Title: SMBUS Routing Table

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 56 of 60

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	change to the latest 2015 for MOSFET application.	01	45	change PQ305 to MDV1528 & PQ306 MDV1527		EVT
02	Design Change.	change to the latest 2015 for MOSFET application.	01	47	change PQ503 to MDV1528		EVT
03	Design Change.	change to the latest 2015 for MOSFET application.	01	51	change PQ9002 & PQ9005 to MDU1516		EVT
04	Design Change.	change to the latest 2015 for MOSFET application.	01	51	change PQ9001, PQ9003, PQ9007 & PQ9009 to MDV1511		EVT
05	Design Change.	change to the latest 2015 for MOSFET application.	01	57	change PQ1201 & PQ1203 to MDU1516		EVT
06	Design Change.	change to the latest 2015 for MOSFET application.	01	57	change PQ1202 & PQ1204 to MDU1511		EVT
07	power off pulse issue when S0 -> S5.	+0.675VS have a pulse when S0->S5 as attached.	01	47	change Pu501 8207P to 8207M		EVT
08	power off pulse issue when S0 -> S5.	8207M output cap is use 330uF poscap	01	47	Delete PC510~PC515 22u*6		EVT
09	power off pulse issue when S0 -> S5.	8207M output cap is use 330uF poscap	01	47	Add PC510 330u*1		EVT
10	power off pulse issue when S0 -> S5.	8207M frequency is different with 8207P	02	47	change PR507 to 887k ohm		DVT
11	Design Change.	Tune +1.5VSDGPUP enable time	02	53	change PR1002 to 40.2k ohm		DVT
12	Stop use Anpec LDO	Anpec LDO is EOL	02	49	change Pu702 to G971		DVT
13	DFB request	pin is too small, avoid open solder	02	44	Change PJP201 SP021210250 (ACES_50458-00801-001_8P-T) to SP020017H00 (CVILU_CI9908M2HR0-NH_8P)		DVT
14	Tune CPU transient	Tune CPU transient	02	50	Change PR808 to 24.9k ohm PR822 to 24.9k ohm PR846 to 2.4k ohm PR867 to 2.4k ohm PR842 to 36.5k ohm PR836 to 69.8k ohm PR859 to 10k ohm		DVT
15	Design Change.		02	45	Change PC315 0.1u to 2200p		DVT
16	Design Change.	change 1V output from 1.011V to 1.02V	02	48	Change PR608 13.7k to 14k ohm		DVT
17	Tune CPU transient	Tune CPU transient	02	50	Change PR846 to 2.43k ohm PR867 to 2.43k ohm PR836 to 71.5k ohm		DVT
18	Design Change	Change to common part	02	53	Change PL9002, PL9003, PL1001 & PL1201 to common part (HCB2012KF-121T50_0805)		DVT
19	thermal request	change PH1 from 92degree to 89degree	02	44	Change PR204 from 16.9k ohm to 18.7k ohm		

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Compal Electronics, Inc.

Title: PIR

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	11	CPU	1/9	NA	Reserved RC189(0 ohm) for DGPU_AC_DETECT	DVT	0.2
2	38	EC	1/9	Reserved protect circuit when adaptor 107% happen, requrie from Acer	Change net from VCOUT1_PROCHOT# to VCOUT1_PROCHOT Change U4901.117 from SEN_DET# to SW_PROCHOT# Reserved Q2010A/B for SW_PROCHOT# and DGPU_AC_DETECT Add R4960 for SW_PROCHOT# and VCOUT1_PROCHOT Rename R4938.2 to SW_PROCHOT#	DVT	0.2
3	38	EC	1/9	Remove unuse part	Delete R4905, R619, R4958	DVT	0.2
4	10	CPU	1/12	SYS_RESET# Pull-up to ALWAYS power rails	Change RPC11.6 to +3VALW_PRIM	DVT	0.2
5	11	CPU	1/12	Reserved PD for G_INT#	Reserved RC117 for G_INT#	DVT	0.2
6	11	CPU	1/12	NA	Move RC212 to Page06 and add note for EC_SCI#	DVT	0.2
7	11	CPU	1/12	Separate RPC18 for easy PU	Change RPC18 to RC126, RC127 (1K) and RC128, RC129 (2.2K)	DVT	0.2
8	17	CPU	1/12	Reserved for Cannonlake-U (2014MOW52)	Connect UC1.U11/U12 to +1.8VALW_PRIM and reserved CC79 for UC1.U11/U12	DVT	0.2
9	18, 19	Memory	1/12	Change CIS Symbol and Footprint	Change CD16,CD46 PN to SGA00009S00	DVT	0.2
10	29, 37	USB	1/12	Change CIS Symbol and Footprint	Change L24,L25,L26,L28,L29,L30, L27 CIS Symbol to SM070003Y00	DVT	0.2
11	33	LAN	1/12	Reserved path for +3V_LAN	Reserved R214 0_0850 for +3V_LAN	DVT	0.2
12	35	WLAN	1/12	Disconnect SUSCK to M.2 connector to avoid leakage current	R426 change to 0_0402 @	DVT	0.2
13	37, 38	USB	1/12	Control USB Charger behavior when disabel USB charger funct i on	Change R854.1 from SUSP# to USB_CB and U4901.70 from OPMODE to USB_CB	DVT	0.2
14	38	EC	1/12	Board ID change to DVT	Change R4903 from 0_0402_5% to 12K_0402_5%	DVT	0.2
15	38	EC	1/12	Remove unuse part	Delete R4957, R4959	DVT	0.2
16	39	LED	1/12	LED light adjust	Change R3 to 560 ohm and change R6 to 430 ohm Change R2633.2 to +3VLP	DVT	0.2
17	39	LID	1/12	Change Hall Sensor IC	Change U3 to SA00008K800 (ANPEC)	DVT	0.2
18	39 11	PTP	1/12	Add level shift for PTP I2C interface	Add Q2012A/B, R2641, R2642, R2639, R2640 Change RC128,RC129 PU to +3VALW_PGPPC	DVT	0.2
19	41	Others	1/12	Follow DFX requriement	Change H17 from 3P2 to 3P3	DVT	0.2
20	42	Sequence	1/12	For power off sequence	Add R1000, R1002, Q2013, Q2014, Q2016 for tCPU17, tCPU18, tCPU28, tPLT15	DVT	0.2
21	06	Debug	1/15	Reserved for power on select	Reserved RC53, RC54 for JAPS1.11	DVT	0.2
22	36	HDD	1/15	Pin def i nit on modf y	JHDD2.10 connect to GND	DVT	0.2
23	39	Others	1/15	Pin def i nit on modf y	JLID1.2 change to LID_SW#, JLID1.3 NC	DVT	0.2
24	08	SPI	1/20	Remove/Un-Pop unuse part	Del RC203 and change un-pop RPC6	DVT	0.2
25	09, 40	DMIC	1/20	Reserved DMIC path from SOC	Reserved R481, R482 for PCH_DMIC_CLK/DATA from UC1.H5/D7 Add R483, R484 0_0402 for Audio DMIC	DVT	0.2
26	22	NV	1/20	Update HYNIX C die straps table	Update HYNIX C die straps table	DVT	0.2
27	30	Others	1/20	Remove unuse part	Del R377, R378, R376	DVT	0.2
28	35	WLAN	1/20	Separate M.2 pin32 and 46 for Intel WLAN 3165	JNGFF1.32 change to NC (for Intel 3165)	DVT	0.2
29	38	Sequence	1/20	For power down sequence	Add D27 for EC_VCCST_PG_R	DVT	0.2
30	39	LED	1/20	Update CIS Symbol and Footprint	Update LED1, LED2 CIS Symbol	DVT	0.2
31	40	Audio	1/20	Update BOM Structure	Change R2135, R2151 to EMC@	DVT	0.2
32	40	Audio	1/20	Adjust MONO_IN input voltage	Change R2140 to 27K and R2138 to 27K(@)	DVT	0.2
33	41	Others	1/20	Change reset signal	Mount R2631 and un-mount R2632	DVT	0.2
34		Others	1/20	Change 0 ohm to R-Short	0_0603 to R-Short: R2075, R81, RC176, RC209 0_0402 to R-Short: R2131, RC172, R472, R927, R2552, R4953, R4956, RC178, RC197, R427,R428	DVT	0.2
35	20	NV	1/28	Remove unuse part	Del D2002, R2055	DVT	0.2
36	30	HDMI	1/28	Remove unuse part	DEL ZZZ1 (HDMI ROYALTY)	DVT	0.2
37	30	HDMI	1/28	Change U52 main source (HDMI power switch)	U52 change to SA00004ZA00	DVT	0.2
38	38	EC	1/28	Un-use part change to @	R4943 change to @	DVT	0.2
40	06	CMC	2/4	Change XDP to CMC	Change JXDP1 CIS symbol to CMC CIS Symbol(JPCMC1) Del RPC3, RC22, RC25, RC20, RC14, CC120, CC121, RPC4 Rerout i ng RPC2, RPC4, RPC15, RC23, RC151 Add RC17, RC55, RC56 Change RC37 to @ Change XDP@ to CMC@	DVT	0.2
41	08	LPC	2/4	Change 0 ohm to R-Short	Change RPC8 to RC144~ RC147 0 ohm R-short	DVT	0.2

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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PIR-HW1

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
42	10		2/4	Remove unuse part	Del RC108	DVT	0.2
43	10	SOC	2/4	Add T164/T165 for CLK_CPU_ITP/CLK_CPU_ITP#	Add T164/T165 for CLK_CPU_ITP/CLK_CPU_ITP#	DVT	0.2
44	10	SOC	2/4	Change Material of AND gate	Change UC3 to SA00000OH00	DVT	0.2
45	12	SOC	2/4	Follow PCH EDS1.2 add PD resistor when un-use USB	Add RC130, RC131 for USB2_ID and USB2_VBUSSENSE	DVT	0.2
46	10	SOC	2/5	Reserved PD resistor (2014MOW48)	Reserved RC136 for Cannonlake-U	DVT	0.2
47	13	SOC	2/5	Reserved path for VCCIO	Reserved U4902, C977	DVT	0.2
48	06	SOC	2/9	Reserved path for TP_INT#	Reserved RC137	DVT	0.2
49	17	SOC	2/9	Reserved power source for U11/U12	Add RC57 for UC1.U11/U12	DVT	0.2
50	19	DIMM	2/9	Remove un-use part	Del CD46	DVT	0.2
51	29,37	USB Chock	2/9	Swap net because update CIS Symbol	SWAP net of L24,L25,L26,L28,L29,L30,L27	DVT	0.2
52	10	Crystal	2/11	Update 32.768KHz Crystal to 9pF	Change YC2 PN to SJ10000L000	DVT	0.2
53	41	D-Cover	2/25	Reserved SW5 for memory door on D-Cover	Reserved SW5(@)	DVT	0.2
54	14	PCH	2/26	Reserved for Intel PDG1.2 Table52-9	Reserved CC123, CC124,CC125	DVT	0.2
55	40	DMIC	3/2	Follow PDG1.2 Table28-3	R481,R482 change to 33 ohm	DVT	0.2
56	08	SPI	3/3	2015MOW06 no need PU1K on SPI_IO2/IO3	Un-Mount RC47	DVT	0.2
57	08	Crystal	3/3	Modify for 9pF Cyrstal	Change CC15,CC16 to 8.2pF	DVT	0.2
58	18,19	Memory	3/3	Mount decoupling capacitor	Mount and change CD1, CD17, CD28, CD47 to 0.1U_0402	DVT	0.2
59	35	SUSCLK	3/3	Del SUSCLK and reserved TP(Reqruie from Acer)	Del R426, C85 and add T3806	DVT	0.2
60	39	Others	3/3	Un-mount un-use part	Un-mount SW3	DVT	0.2
61	08	SMBUS	3/3	Add level shift for SOC_SMBCLK/SOC_SMBDATA	change RC202, RC49, RC50, RPC7 PU to +3VALW_PRIM add Q2017, RC220, RC221, RC222, RC223 change net name from SOC_SMBCLK/SOC_SMBDATA to SOC_SMBCLK_1/SOC_SMBDATA_1 change RPC7 PU to 2.2K	DVT	0.2
62	08	Others	4/1	Delete reserved component	Del RPC8, RC45, RPC6	PVT	0.3
63	08	SMBUS	4/1	Add BOM Structure for SPI ROM	Change RPC5 and RC52 to 15 ohm with 8M_SINGLE@ Add RPC5 and RC52 33 ohm with 8M_DUAL@ Add reserved component UC2 with 8M_DUAL@	PVT	0.3
64	08	SMBUS	4/1	Delete EC SPI path	Del RPC6	PVT	0.3
65	08	SPI	4/1	MOW36 QS sample no need to PD	Change RC51 to ES@	PVT	0.3
66	13,39,41	Others	4/1	Change 0 ohm to R-Short	0_0402 to R-Short: R2631, R2634, RC168, RC186	PVT	0.3
67	37	Others	4/1	SMT require delete un-use 0 ohm to avoid USB chock solder issue	Del R458, R461, R465, R466	PVT	0.3
68	38	LID	4/1	For 2nd source hall sensor soultion	Mount R618	PVT	0.3
69	30,31	Others	4/1	PD for HPD signal	Add R380 PD100K, Mount R2530	PVT	0.3
70	38	Others	4/1	Board ID Change for PVT	change R4903 to 15K	PVT	0.3
71	42	Others	4/8	Add discharge circuit for +1.05VSDGPU	Mount Q2008, R574, R1001	PVT	0.3
72	30,37,40	Others	4/14	Change 0 ohm to R-Short	0_0402 to R-Short: R368,R369, R370, R371, R372,R373, R374, R375 R473, R474, R475, R476, R477, R478, R479, R480 0_0603 to R-Short: R2135, R2151	PVT	0.3
73	37,38	Others	4/16	Change U77 pin4 control by EC GPIO	link U77.4 to U4901.119 Un-mount R857	PVT	0.3
74	12	CPU	4/17	Follow MOW10, USB2_ID/USB2_VBUSSENSE connect to GND	Change RC130, RC131 to 0 ohm	PVT	0.3
75	40	Audio	4/17	Beep Sound Path from EC	Change R2138, R2140 to 22K and mount R2138	PVT	0.3
76	06	CPU	4/22	Add test point for CATERR#	Add T166	PVT	0.3
77	06	Others	4/22	Cancel JAPS1 Mask to avoide soldering issue	change JAPS1 footprint to ACES_50506-01841-P01_18P-NPM	PVT	0.3
78	22, 25	GPU	4/30	Add Samsung E-Die VRAM Information	Add X76629BOL13/X76629BOL14	PVT	0.3
79	03, 07	CPU	4/30	Add QS sample CPU for BOM Selection	Add UC1 with QJFC@/QJ8N@/QJ8L@	PVT	0.3

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
80	42	Others	5/14	BOM Error	Change R574, R1001, Q2008 to VGA@	Pre-MP	1.0
81	38	Others	5/28	For abnormal shutdown	Mount D26	Pre-MP	1.0
82	38	Others	5/28	Board ID change to Rev1.0	Change R4903 to 20K_0402_1%	Pre-MP	1.0
83	01	Others	6/17	Update PCB Rev10 PN	Update PCB PN to DAZ1DR00100	Pre-MP	1.0
84	39	Others	6/22	Cancel the MASK of JLID1	Change JLID1 to ACES_50506-01041-P01_10P-NPM	Pre-MP	1.0
85	38	Others	7/14	Add C4917 for EC_RST#	Add C4917	Pre-MP	1.0
86	39	Others	7/14	Add S spec number for i3/i5/i7 CPU	add SR2EU@/SR2EY@/SR2EZ@ for UC1 MP number	Pre-MP	1.0

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